Design of a 100 MHz, 5th Order Elliptic, Low-Pass Switched Capacitor Filter

Jon Guerber, ECE 626, *Student Member, IEEE*

***Abstract*—The design and simulation of an Elliptic switched capacitor filter with modeled non-idealities will be discussed and analyzed. The complete design procedure starting with specifications will be shown. Non-idealities such as finite bandwidth, charge injection, slew rate, offset, finite gain and real world opamps have been incorporated into this study and their effect will be demonstrated though simulation. Finally dynamic range scaling and chip area scaling will be examined for optimal design.**

I. Introduction

Since the dawn of the electronics, the physical laws of nature have necessitated a way to remove unwanted noise from a desired signal. The filter was created to mitigate this problem and has evolved from crude passive device configurations to highly modeled continuous and discrete time integrated blocks. Currently, many low frequency filters employ switched capacitor methods due to the high predictability, reduced cost, and ease of design.

In this paper, a switched capacitor filter with a sampling frequency of 100 MHz has been designed. This filter is designed without phase considerations, assuming that its use will be in delay tolerant systems or will be followed by an all-pass phase correcting filter. The design is for a minimum passband ripple of .2dB at 5 MHz and a stopband attenuation of 50 db at 10 MHz. The result is simulated in Cadence Composer and has been modeled with many non-idealities and real opamp designs. The paper will be constructed as follows: Section 2 will feature the design methodology for a switch capacitor filter based on the given specifications, Section 3 will feature actual schematic simulations and dynamic range scaling, Section 4 will discuss non-idealities of a switched capacitor filter, Section 5 will discuss the filter response with real opamps, and Sections 6 will draw some conclusions about the design of the filter. Code and further resources can be found in the appendix.

II. Switched Capacitor Filter Design Methodology

A. Filter Topology Choice

The first step in the design of any filter is what topology should be chosen. Due to simplicity and debug-ability, it was determined that a cascade of biquads and a possible liner filter section would be desired. The order of this filter would be determined by the filter specifications as shown in Table 1.

Manuscript received March 16, 2009.

J. Guerber is with the Oregon State University, Analog and Mixed Signal Department, Corvallis, OR 97330 USA (e-mail:guerberj@ eecs.orst.edu).

TABLE I
Filter Design Specifications

Parameter	Specified Value
Sampling Frequency	100 MHz
DC Gain	0 dB
Passband Frequency	0-5 MHz
Ripple in Passband	< 0.2 dB
Stopband Frequency	10-50 MHz
Gain in Stopband	< -50 dB
Minimum Capacitor Size	0.05 pF

With use of Matlab filter design tools, we can quickly compare the relative order of the filter for the specifications above. These filter order results are shown in Table 2.

TABLE II
Filter Order Requirements

Filter Type	Minimum Order
Butterworth	11
Chebyshev Type I	6
Chebyshev Type II	6
Elliptic	5

Since there are no phase considerations, the most area efficient choice would be the 5th order elliptic configuration. This elliptic filter was first designed in the S-domain and then transformed to the Z-domain using the bilinear transform. This was determined to be highly accurate since there are few high frequency poles in this design. Equation 1 shows the final transfer function for this filter design.

$$H(z)=\frac{(.003346)z^5-(.007239)z^4-(.004402)z^3+(.004402)z^2-(.007239)z+.003346}{z^5-4.393z^4+7.856z^3-7.137z^2+3.29z-.6151}$$

Equation 1: Elliptic Filter Transfer Function

B. Ideal Filter Response

It is important that the transfer function response be verified before this function will be implemented in a real circuit design.

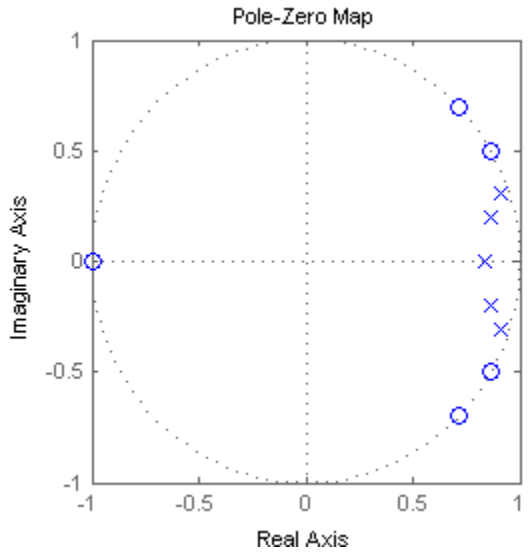

Figure 1: Filter Poles and Zeros

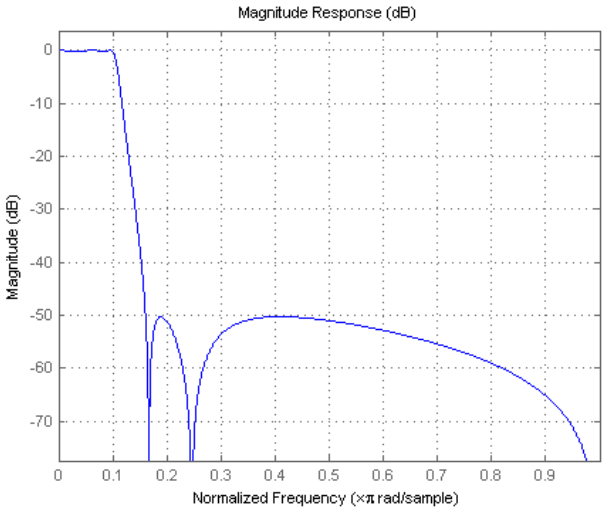

Figure 2: Filter Magnitude Frequency Response

This can be done by plotting the pole and zero location, examining the transient impulse response and verifying that the frequency magnitude response of the filter matches the specifications.

Figure 1 shows the location of the poles and zeros for the filter transfer function described by Equation 1. This plot displays the characteristic pole and zero locations with a high and low Q pole. Since this is an odd-order filter there is a pole on the real axis and a zero at the nyquist frequency.

Figure 2 shows the filter magnitude response of the transfer function described by Equation 1. This verifies that this transfer function has a stopband below -50 dB for frequencies above 10 MHz (20% of the normalized frequency). Figure 3 shows the ripple in the passband of the filter which is below .2 dB.

The transient response of the filter can also be important for many applications. Shown in Figure 4 is the step response of the filter which can be compared with the transient response of the actual circuit for functionality.

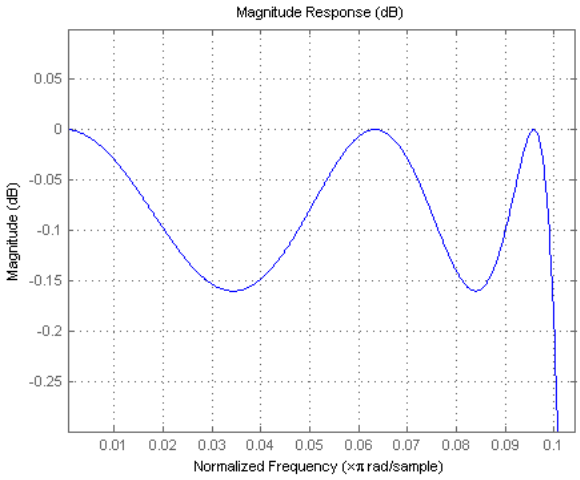

Figure 3: Filter Passband Magnitude Response

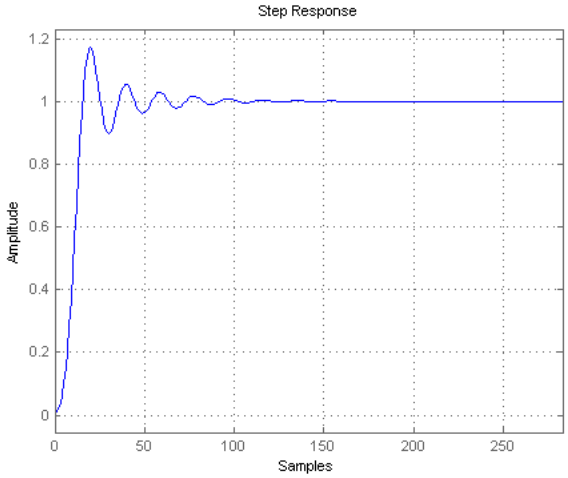

Figure 4: Filter Step Response

C. The Design of Filter Sections

Since the characteristics of the transfer function have been determined, the individual biquads and linier section functions must be found. Using a Matlab tool called "SOS", the respective sections can be easily derived. Equation 2 shows the lowpass first order section which will be the first in the cascade of filter sections. Equation 3 and Equation 4 are biquads with Q's of 5.02 and 1.1 respectively.

$$H(z_L) = \frac{z+1}{z-.8436}$$

Equation 2: Linear Section Transfer Function

$$H(z_{HQ}) = \frac{z^2 - 1.7418z + 1}{z^2 - 1.8327z + .9365}$$

Equation 3: Biquad Transfer Function (Q = 5.02)

$$H(z_{LQ}) = \frac{z^2 - 1.4533z + 1}{z^2 - 1.7382z + .7967}$$

Equation 4: Biquad Transfer Function (Q = 1.1)

III. Filter Block Implementation

A. Filter Architecture

There are many potential designs for switched capacitor biquads. For this project the linier section and low-Q biquad were designed using traditional parasitic insensitive architectures shown in Figure 5 and Figure 6 respectively. The high Q section was designed using a special structure from [1] that reduces chip area for high Q biquads and is shown in Figure 8. These sections have been cascaded in the order shown in Figure 7 to allow for the low pass filtering of the linear section and the output stability of the low-Q section.

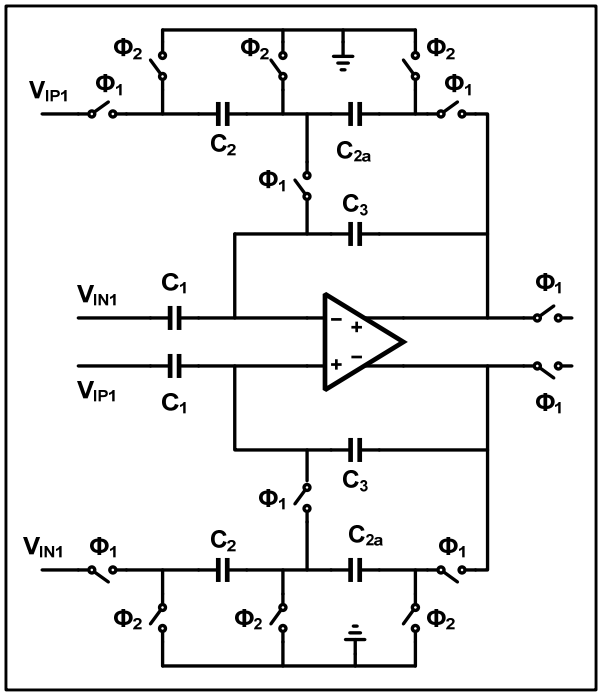

Figure 5: Linear Filter Section

TABLE III
FILTER CAPACITOR VALUES

Capacitor	Calculated Value (pF)	After Dynamic Range Scaling (pF)	After Chip Area Scaling (pF)
C1	1.7865071044	1.2570000000	0.0500000000
C2	3.5730142089	2.5140000000	0.1000000000
C2a	1.9445116853	1.9445116853	0.0773473224
C3	10.0000000000	10.0000000000	0.3977724741
C4	3.9176369828	3.8784606102	0.1031575520
C5	2.7560987890	2.7560987890	0.0733054767
C6	10.0000000000	17.5800000000	0.4675849379
C7	2.7560987900	4.8452216710	0.1288710281
C8	2.6957049130	2.6957049100	0.0716991475
C9	10.0000000000	10.0000000000	0.2659755051
C10	1.8988609680	1.8798723583	0.0500000000
C11	1.2386742820	3.2173994630	0.0782756409
C12	1.4956719466	3.8849390800	0.0945161146
C13	3.2029186740	3.2029186741	0.0779233399
C14	10.0000000000	9.2336103000	0.2246431543
C15	3.2352713880	2.9873235300	0.0726781572
C16	10.0000000000	9.9000000000	0.2408556518
C17	2.0551728656	2.0551728650	0.0500000000

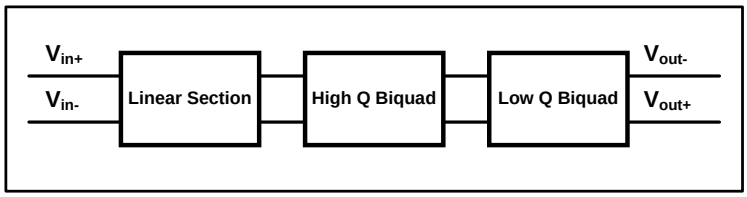

Figure 7: Filter Section Order

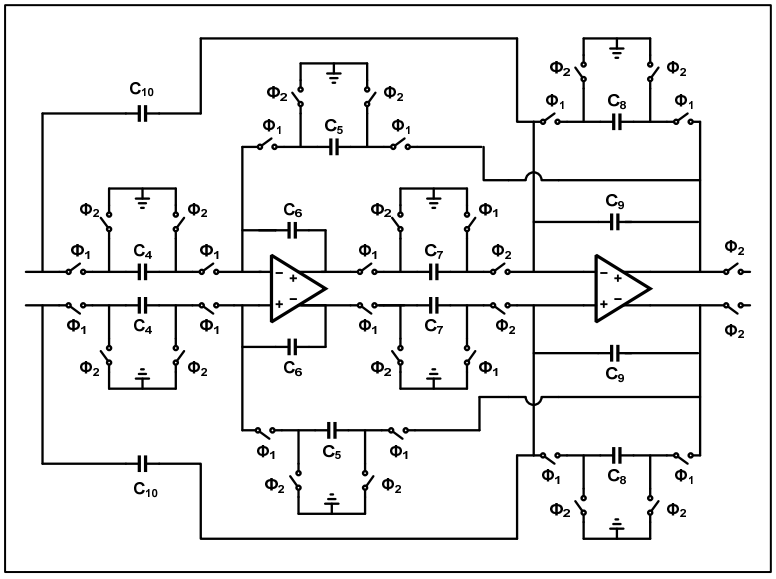

Figure 6: Low-Q Biquad Section

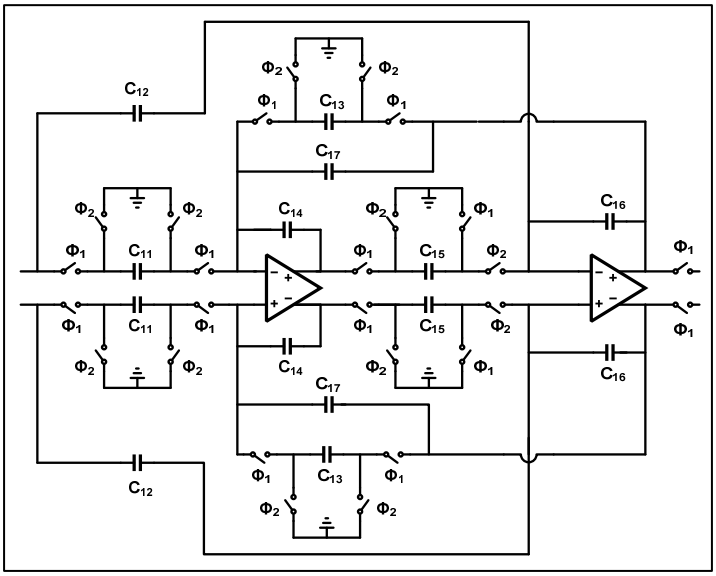

Figure 8: High-Q Biquad Section

B. Simulation Results

The filter coefficients for each of the respective sections were determined by examining the transfer function of each stage and setting one of the parameters arbitrarily to 10p. The filter was then simulated in Cadence using ideal Opamp and Switch models (ideal Opamp is shown in Figure 9). With the selected coefficients, the simulated results show exactly what would be expected with minimal additional passband ripple as shown in Figure 10and Figure 12.

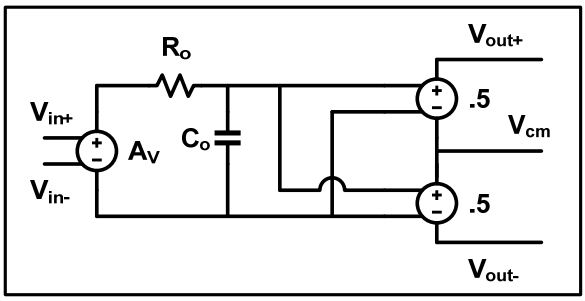

Figure 9: Ideal Opamp Model

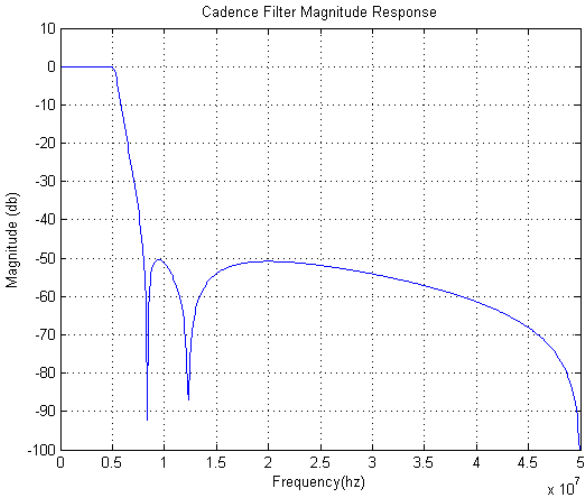

Figure 10: Cadence Simulated Filter Magnitude Response

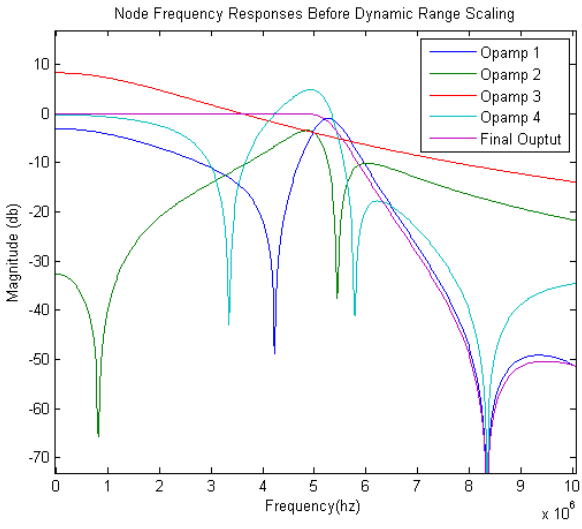

Figure 11: Node Voltages Before Dynamic Range Scaling

C. Dynamic Range Scaling and Chip Area Scaling

After the filter coefficients have been found there are still two degrees of freedom in the capacitance values of the filter that can be used to improve the dynamic range and chip area of the filter. Increasing the dynamic range, or the swing at the output of each opamp will improve the overall SNR by increasing the signal range. This can be accomplished by multiplying the output node capacitors of each opamp by a factor that makes the overall node voltage reach unity. Figure 11 and Figure 13 show the node voltages on the output of every opamp before and after dynamic range scaling.

Chip area scaling is preformed to decrease the area of the overall chip capacitance. This scaling is done by finding the smallest capacitor in each of the filter sub-blocks and finding the dividing factor required to equate that capacitance to the minimum of 50 fF. The scaled coefficients can be found in table 3. After chip area scaling, the effective chip area for capacitors would be the equivalent of a 2.624 pF capacitor.

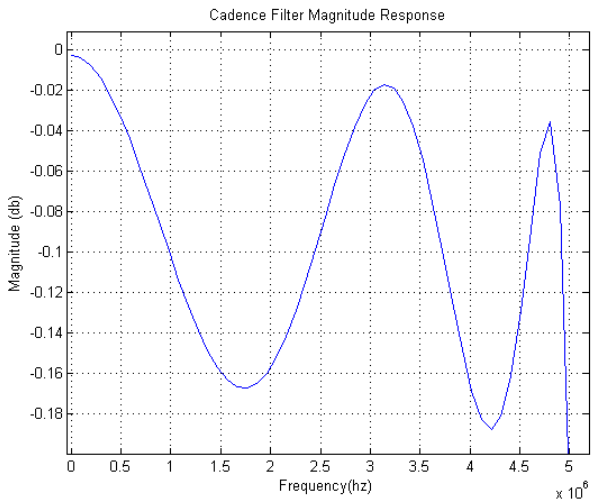

Figure 12: Cadence Simulated Passband Ripple

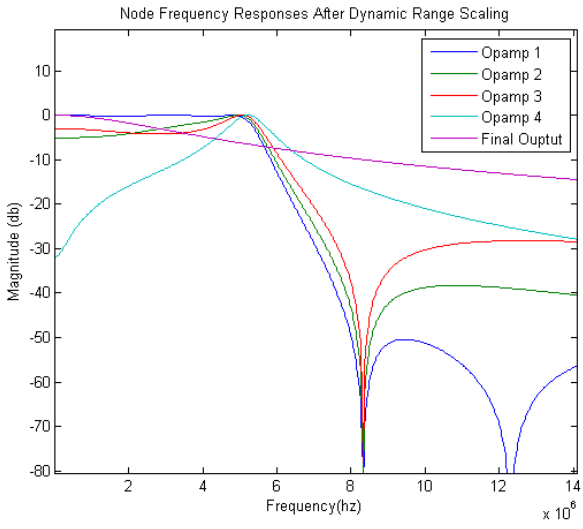

Figure 13: Node Voltages After Dynamic Range Scaling

IV. Switched Capacitor Filter Non-Idealities

All integrated circuits must be designed with the knowledge of how non-idealities will affect the end result in mind. For this filter, the effects of offset voltage, charge injection, slew rate, bandwidth, and finite gain were modeled.

A. *Opamp Offset Voltage*

Offset voltage at the input of an Opamp can be caused by a variety of factors such as mismatch and non-symmetries. In this filter, the effect has been modeled by inserting an ideal voltage source into one of the input terminals of each Opamp. For a given offset voltage, the output skew resulting on the Opamp is shown in Equation 5 to a first order based on the closed loop gain.

$$\Delta V_{Out} = \frac{A_v(V_{Off})}{1 + fA_v}$$

Equation 5: Opamp Skew Given an Input Offset

The filter magnitude response for varying degrees of Opamp input offset can be seen in Figure 14 and Figure 16. It should be noted that the magnitude response becomes noticeably skewed with even small amounts on input offset. If it were not for the feedback loop around the opamp however, even nano-volts of offset could be potential problems.

B. *Charge Injection*

Charge Injection is the phenomena of charge that is stored in the depletion region of a transistor escaping to the surrounding nodes when switched off and absorbing charge when switched on. The amount charge that gets transferred is highly dependent on the depletion region size and capacitance. This can be modeled to a first order by Equation 6.

$$Q_{CH} = -WLC_{OX}(V_{GS} - V_T)$$

Equation 6: Approximation of Channel Charge in NMOS Device

The charge injection into any node can be further approximated as half the channel charge of the active devices. To model this in the switched capacitor filter, a real transmission gate switch has been designed. In real circuits, a bootstrapped switch should be used to eliminate signal dependent charge, however, for modeling purposes, a transmission gate as shown in Figure 15 will work well. The charge injection from the transmission gate switch can determined from Figure 17 to affect the filter output voltage by approximately .015V. Also shown in Figure 19 is the effect of clock feedthrough when the clock goes high on the NMOS (the faster clock). Both while not signal dependent, clock feed though can cause detrimental impulses and will limit the overall clock speed of the circuit.

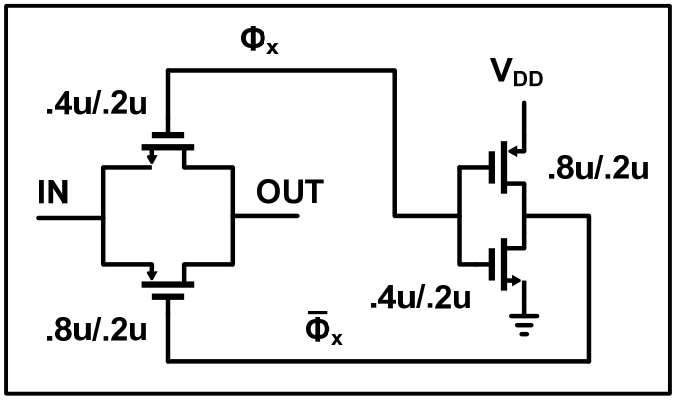

Figure 15: Transmission Gate Used for Modeling Charge Injection

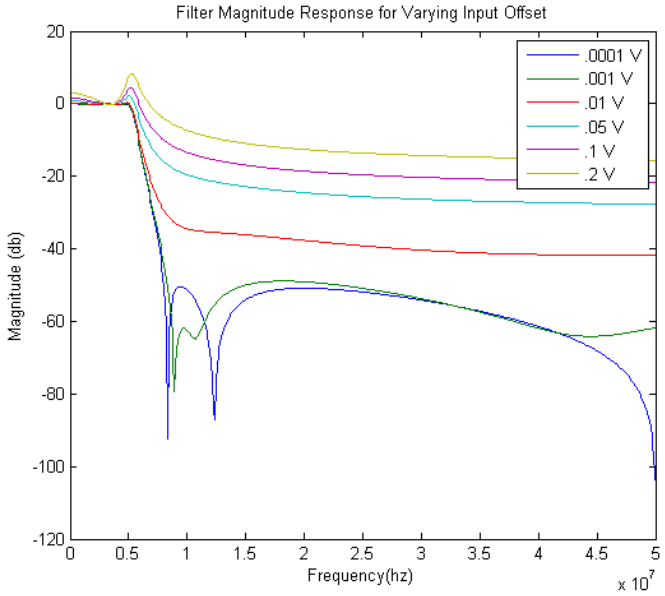

Figure 14: Filter Magnitude Response with Input Offset Voltages

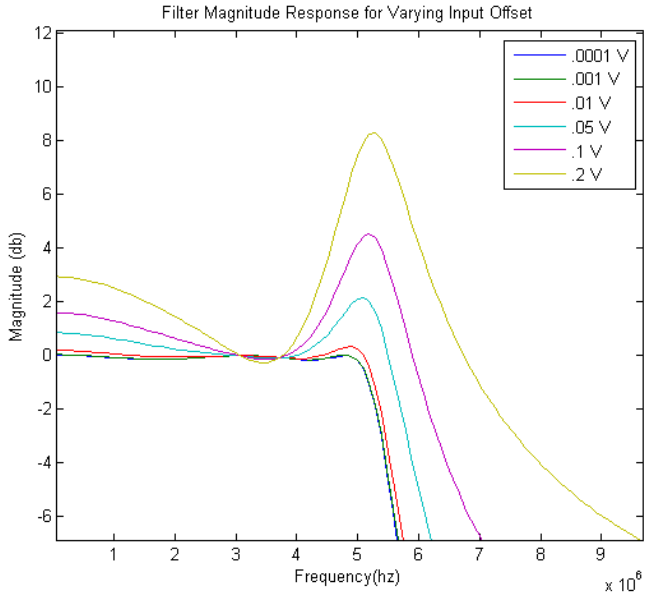

Figure 16: Passband Variation with Input Offset Voltage

C. *Slew Rate*

When designing ideal filters, one would expect the output to respond immediately to any change in the input. However, there is some finite rise time of the output due to the charging and sharing rates among capacitors. The slew rate will be determined by the worst case charging time of the circuit which could be due either to non-ideal opamp current sourcing or switch impedances.

The worst case charging time was determined to come from an ideal pulse applied to the input. Shown in Figure 18 is the slew rate at the output with real switches given an input pulse. The worst case slew rate was determined to be 17.176 v/µs.

D. *Opamp Bandwidth Limitations*

In order to ensure that the settling time of the systems functions properly, the opamp bandwidth should be high enough to ensure that the gain at high frequencies will allow the correct voltages to be resolved by the next phase. The opamp must have at least the nyquist frequency to correctly resolve signal, but in reality needs a bandwidth 5-10 times greater.

Figure 20 shows the effect of finite bandwidth on the frequency magnitude response of the filter. It can be seen that around 100 MHz, the filter begins to decrees its performance as would be expected. Figure 21 shows the passband ripple for decreasing bandwidths.

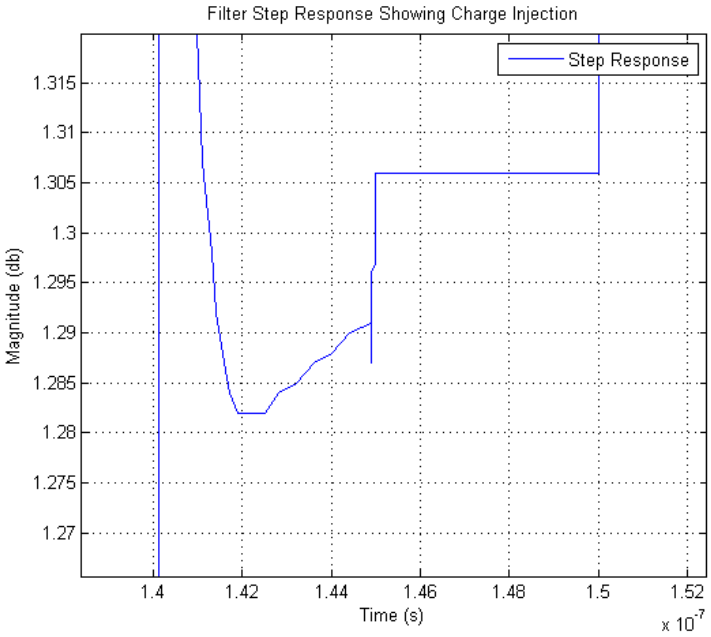

Figure 17: Switch Charge Injection Pedestal

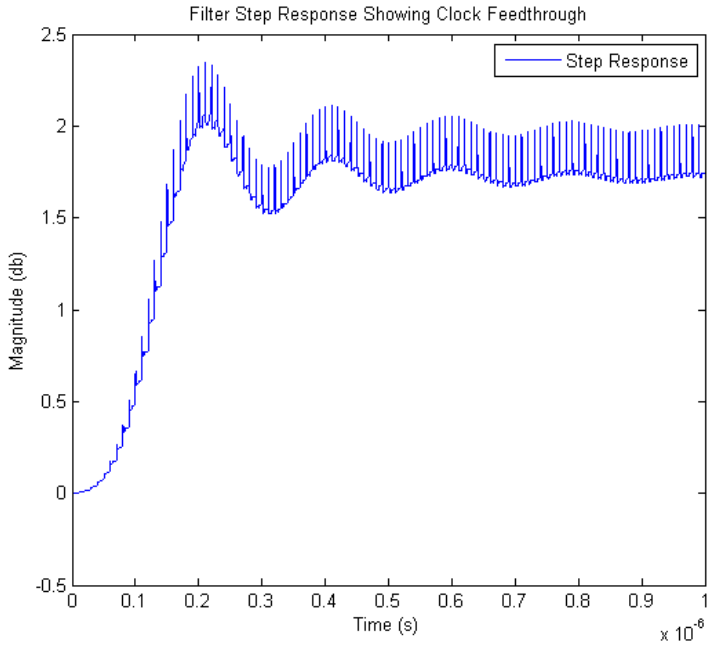

Figure 19: Effect of Clock Feedthrough (Spikes when Switching)

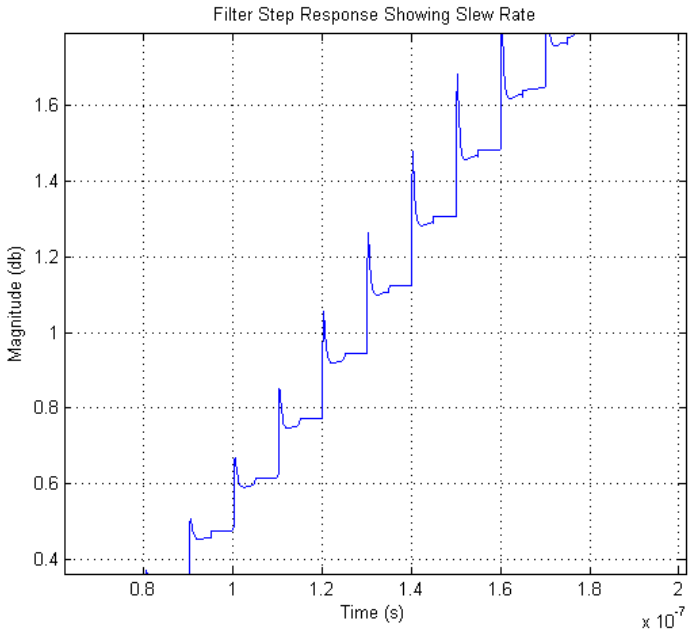

Figure 18: Slew Rate of Filter Output

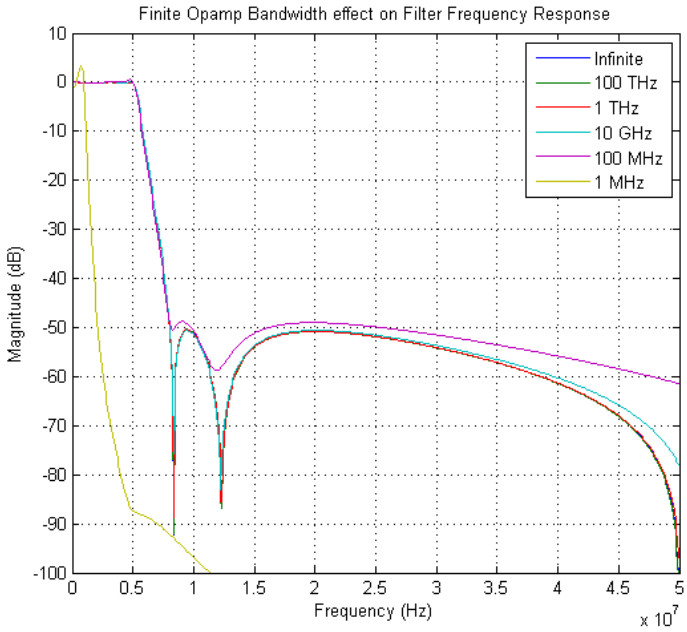

Figure 20: Effect of Finite Bandwidth on Filter Magnitude Response

E. Opamp Finite Gain

If the Opamp in use does not have infinite gain, then the input nodes will not generate a perfect virtual ground node leaving some residual input voltage or gain error. This error will be evident in the actual output of the filter when it becomes high enough as it will restrict the resolving capability of the switched capacitor circuit. Techniques such as correlated double sampling or correlated level shifting can be used to mitigate this problem.

Figure 23 shows the effect of finite opamp gain of the magnitude response of the filter. As would be expected, the finite gain is felt severely around 40db of gain. Figure 22 shows the gain effect in the passband of the filter, which shows similar results from the main response.

V. Switched Capacitor Filter With Real Opamp

In order to accurately model the behavior of the switched capacitor filter under real world conditions, it's essential to model the opamp using real transistor models from fabrication houses. This filter was modeled using TSMC .18 micron devices. The structure of the Opamp is a fully-differential telescopic with gain boosting to maintain a high bandwidth. This opamp has a gain of 125 dB open loop and a unity gain bandwidth of 1 GHz. Figure 24 shows the frequency response of the transistor level filter compared with that of the ideal simulated filter. The response is very well modeled with the only non-ideal opamp elements being 1 current source and some input buffers to prevent input common mode errors. The passband frequency comparison can be seen in Figure 26.

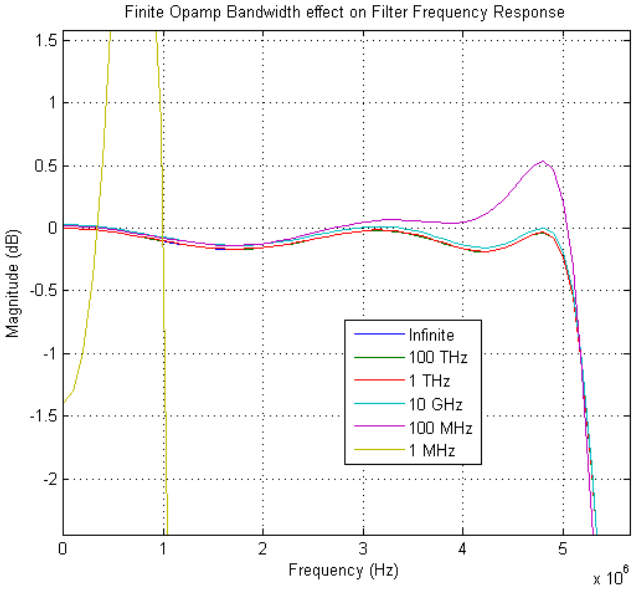

Figure 21: Passband Finite Bandwidth Response

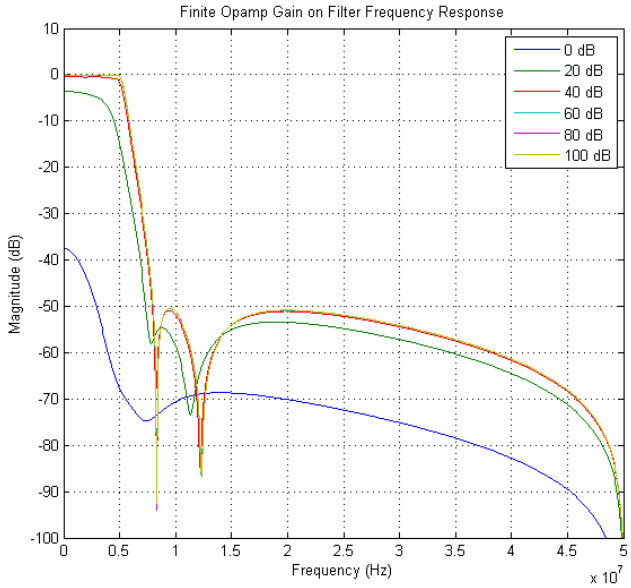

Figure 23: Effect of Finite Opamp Gain on Filter Magnitude Response

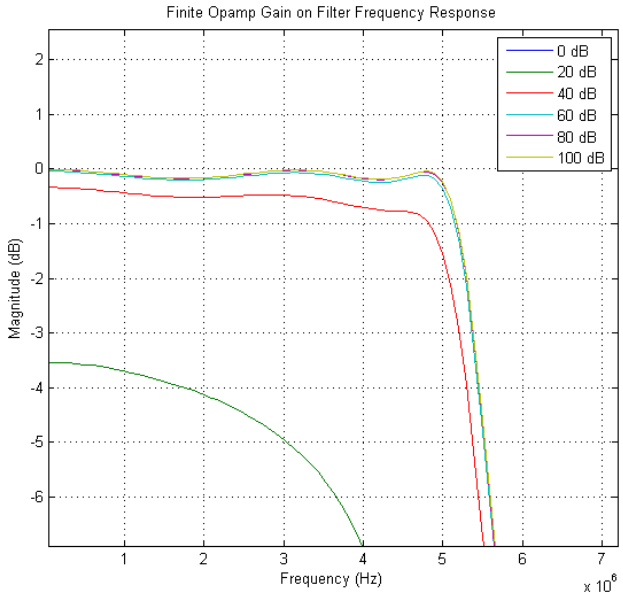

Figure 22: Passband Finite Opamp Gain Response

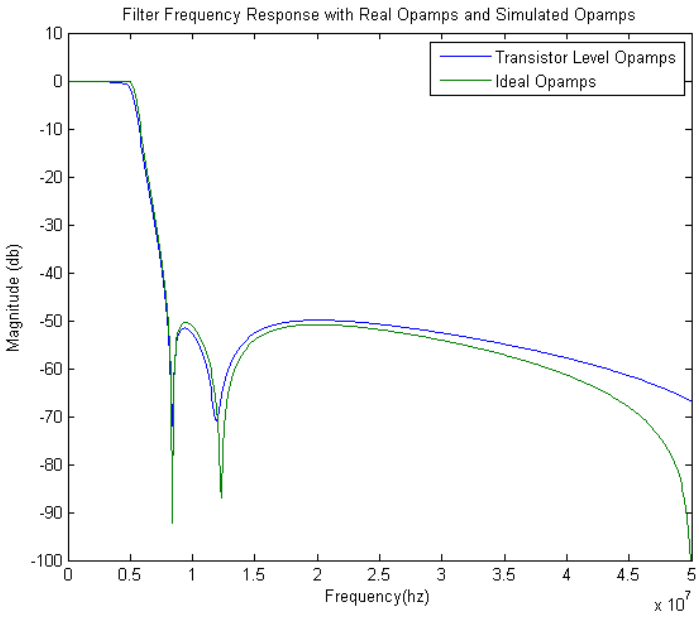

Figure 24: Transistor Level Opamp Filter and Ideal Filter

The design of the transistor level opamp can be seen in Figure 25. This opamp has been created with a main stage gain of about 75 dB with gain boosting providing another 35-45 dB of gain. The telescopic architectures was designed for a high unity gain frequency allowing for reasonable gain even beyond the nyquist frequency. Figure 27 and Figure 28 show the gain boost circuitry and biasing for the real opamp design while Table 4 lists all the device sizes if replication of the circuit is needed. Table 5 shows some simulated Opamp parameters that may be of interest to a filter designer. For additional Opamps simulations results, see the appendix.

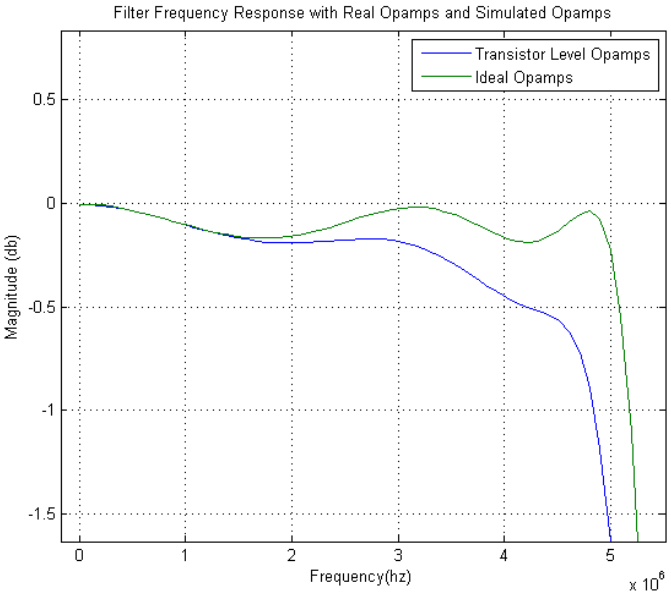

Figure 26: Real and Ideal Opamp Passband Responses

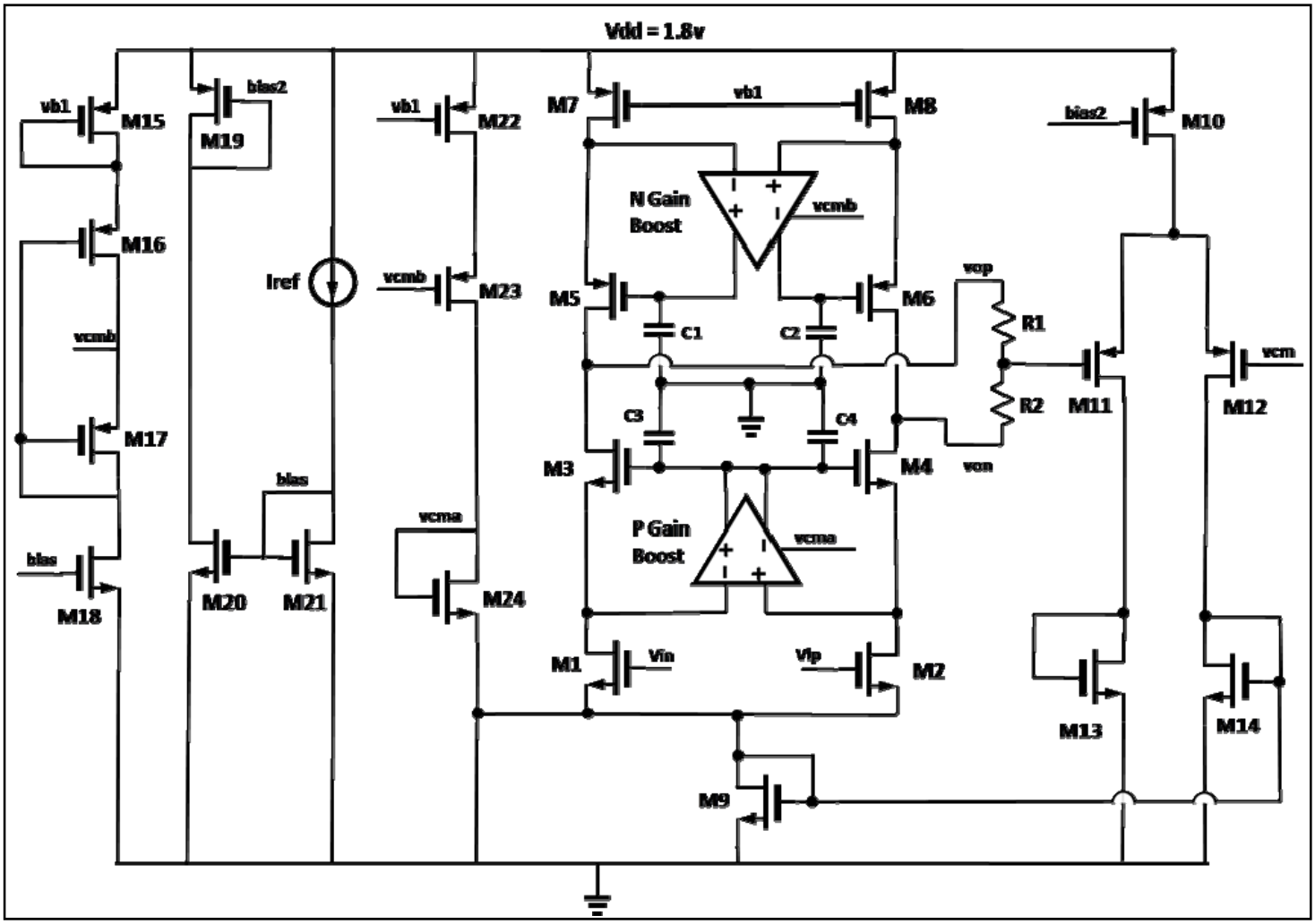

Figure 25: Fully Differential Telescopic Gain Boosted Amplifier used as Transistor Level Opamp

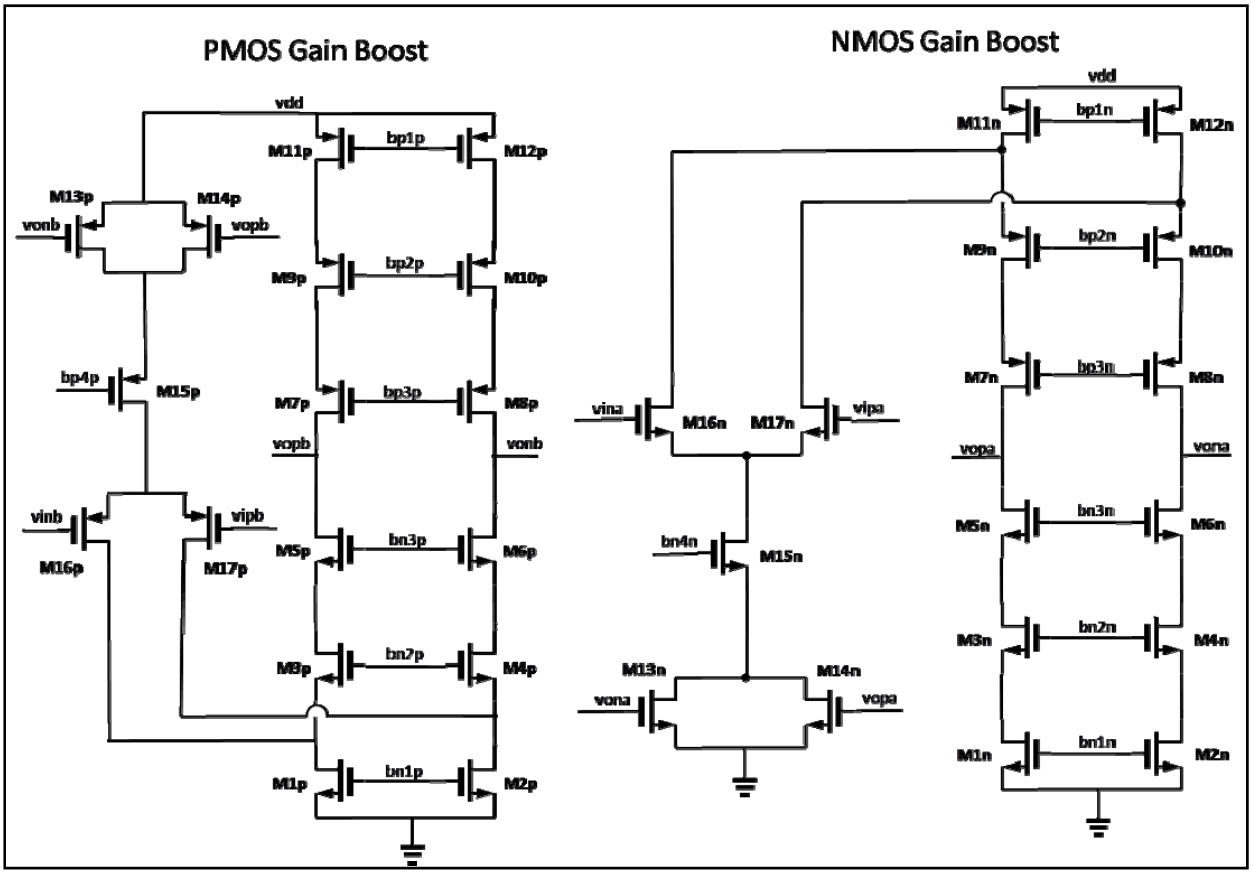

Figure 27: Transistor Level Schematic of Opamp Gain Boosting

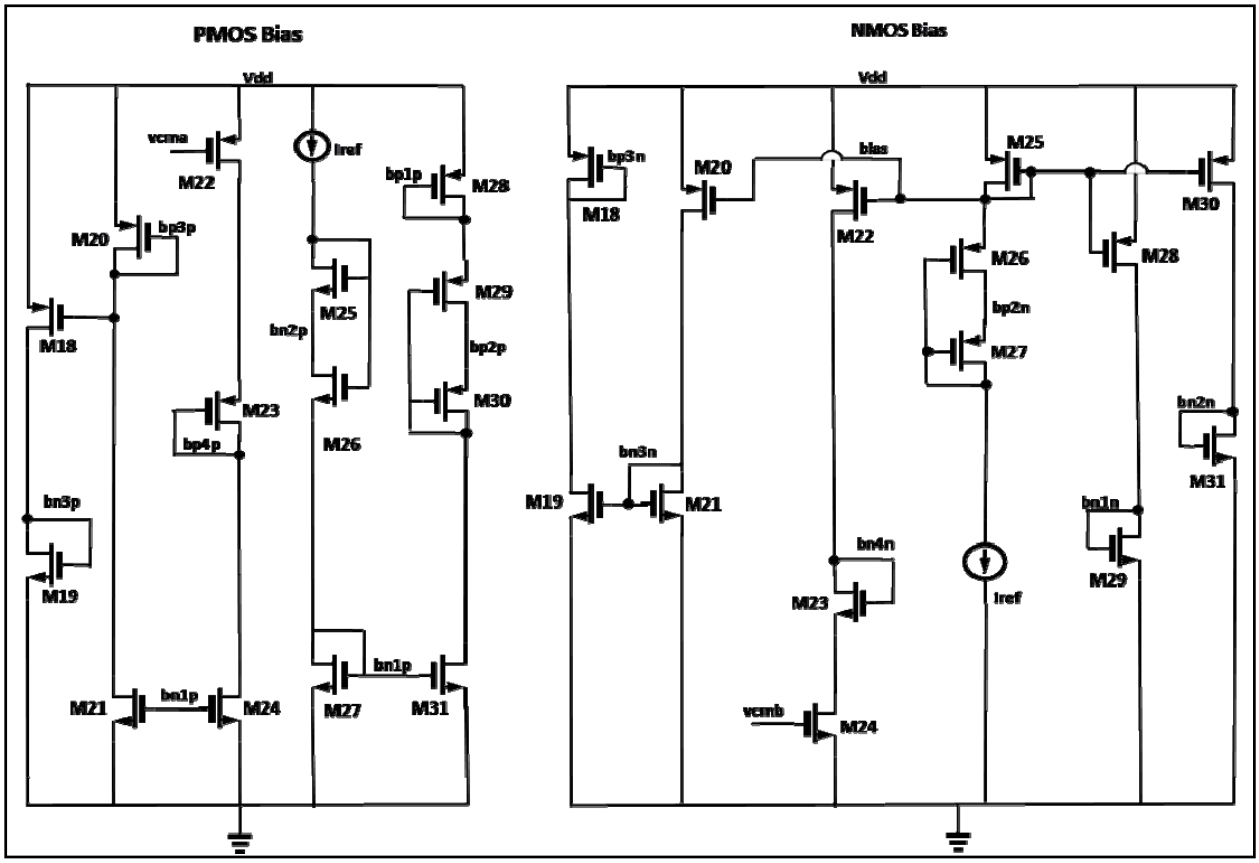

Figure 28: Biasing Circuit for Gain Boosting Sub-Opamps

Table 4:

Device Sizes, Transconductances, currents, and deltas for filter Opamps

Device	Size (W/L)	Bias Current	gm	delta						
Telescopic										
M1	400u/.18u	5.12E-03	7.08E-02	0.14482						
M2	400u/.18u	5.13E-03	7.08E-02	1.45E-01						
M3	400u/.18u	5.13E-03	7.33E-02	0.139921						
M4	400u/.18u	5.13E-03	7.33E-02	0.139921						
M5	1.2m/.18u	5.13E-03	7.08E-02	0.144843						
M6	1.2m/.18u	5.13E-03	7.08E-02	0.144843						
M7	1.2m/.18u	5.13E-03	6.83E-02	0.150146						
M8	1.2m/.18u	5.13E-03	6.83E-02	0.150146						
M9	1.6m/.18u	1.50E-02	2.30E-01	0.130401						
M10	2.6m/.18u	1.18E-02	1.57E-01	0.150605						
M11	1.2m/.18u	2.93E-03	4.80E-02	0.122218						
M12	1.2m/.18u	8.90E-03	9.82E-02	0.181207						
M13	300u/.18u	2.93E-03	5.71E-02	0.102643						
M14	300u/.18u	8.90E-03	1.32E-01	0.135361						
M15	900u/.18u	4.64E-03	5.97E-02	0.155366						
M16	300u/.18u	4.64E-03	2.42E-02	0.384265						
M17	1.2m/.18u	4.68E-03	6.64E-02	0.140985						
M18	400u/.18u	4.64E-03	6.64E-02	0.13978						
M19	1.2m/.18u	6.27E-03	8.00E-02	0.15675						
M20	400u/.18u	6.27E-03	8.02E-02	0.15632						
M21	400u/.18u	5.00E-03	8.02E-02	0.124657						
M22	1.2m/.18u	4.70E-03	6.02E-02	0.156172						
M23	1.2m/.18u	4.72E-03	3.75E-02	0.251733						
M24	14.5u/.18u	4.70E-03	7.01E-03	1.340942						
Iref	5 mA	5 mA								
C1	2 pF	0								
C2	2 pF	0								
C3	2 pF	0								
C4	2 pF	0								
R1	10 G	0								
R2	10 G	0								
NMOS	Size (W/L)	Bias Current	gm	delta		PMOS	Size (W/L)	Bias Current	gm	delta
M1	64u/.36u	7.15E-04	6.93E-03	2.06E-01		M1	233.2u/.18u	1.90E-03	1.00E-02	3.80E-01
M2	64u/.36u	7.15E-04	6.93E-03	0.206322		M2	233.2u/.18u	1.90E-03	1.00E-02	3.80E-01
M3	64u/.36u	7.15E-04	7.34E-03	0.194741		M3	116.6u/.36u	8.87E-04	1.10E-02	1.61E-01
M4	64u/.36u	7.15E-04	7.34E-03	0.194741		M4	116.6u/.36u	8.87E-04	1.10E-02	1.61E-01
M5	64u/.36u	7.15E-04	7.90E-03	0.180937		M5	116.6u/.36u	8.87E-04	1.16E-02	1.53E-01
M6	64u/.36u	7.15E-04	7.90E-03	0.180937		M6	116.6u/.36u	8.87E-04	1.16E-02	1.53E-01
M7	191.78u/.18u	7.14E-04	1.02E-02	0.139603		M7	383.4u/.36u	8.87E-04	1.04E-02	1.71E-01
M8	191.78u/.18u	7.14E-04	1.02E-02	0.139603		M8	383.4u/.36u	8.87E-04	1.04E-02	1.71E-01
M9	191.78u/.18u	7.14E-04	1.03E-02	0.138776		M9	383.4u/.36u	8.87E-04	1.06E-02	1.67E-01
M10	191.78u/.18u	7.14E-04	1.03E-02	0.138776		M10	383.4u/.36u	8.87E-04	1.06E-02	1.67E-01
M11	383.56u/.18u	2.18E-03	2.58E-02	0.169147		M11	383.4u/.36u	8.87E-04	9.25E-03	1.92E-01
M12	383.56u/.18u	2.18E-03	2.58E-02	0.169147		M12	383.4u/.36u	8.87E-04	9.25E-03	1.92E-01
M13	58.3u/.18u	1.46E-03	2.46E-03	1.186992	Triode	M13	191.7u/.18u	1.10E-03	1.36E-02	1.62E-01
M14	58.3u/.18u	1.46E-03	2.46E-03	1.186992	Triode	M14	191.7u/.18u	1.10E-03	1.36E-02	1.62E-01
M15	110u/.18u	2.90E-03	2.99E-02	0.19398		M15	3.83u/.18u	2.20E-03	2.80E-03	1.57E+00
M16	55u/.18u	1.46E-03	1.52E-02	0.192105		M16	1.97u/.18u	1.10E-03	1.36E-02	1.62E-01
M17	55u/.18u	1.46E-03	1.52E-02	0.192105		M17	1.97u/.18u	1.10E-03	1.36E-02	1.62E-01
M18	21.3u/.18u	1.29E-03	3.92E-03	0.658163		M18	18u/.18u	1.08E-03	3.28E-03	6.59E-01
M19	6.47u/.18u	1.29E-03	2.99E-03	0.862876		M19	18u/.18u	1.08E-03	3.28E-03	6.59E-01
M20	191.78u/.18u	1.33E-03	1.51E-02	0.176159		M20	6u/.18u	1.08E-03	2.77E-03	7.80E-01
M21	6.47u/.18u	1.30E-03	3.03E-03	0.858086		M21	18u/.18u	1.12E-03	3.34E-03	6.71E-01
M22	191.7u/.18u	1.50E-03	1.67E-02	0.179641		M22	53.8u/.18u	1.10E-03	1.29E-02	1.71E-01
M23	68.3u/.18u	1.50E-03	1.55E-02	0.193548		M23	191.7u/.18u	2.36E-07	6.00E-06	7.87E-02
M24	68.3u/.18u	1.50E-03	2.45E-03	1.22449		M24	191.7u/.18u	2.36E-07	5.99E-06	7.88E-02
M25	191.78u/.18u	1.30E-03	1.49E-02	0.174497		M25	53.8u/.18u	2.36E-07	1.95E-06	2.42E-01
M26	63.9u/.18u	1.30E-03	5.20E-03	0.5		M26	58.3u/.18u	1.05E-03	1.33E-02	1.58E-01
M27	191.78u/.18u	1.30E-03	1.49E-02	0.174497		M27	15u/.18u	1.05E-03	3.95E-03	5.32E-01
M28	191.78u/.18u	1.52E-03	1.63E-02	0.186593		M28	53.8u/.18u	1.05E-03	1.23E-02	1.71E-01
M29	58.3u/.18u	1.50E-03	1.55E-02	0.193548		M29	191.78u	9.89E-04	1.27E-02	1.56E-01
M30	191.78u/.18u	1.40E-03	1.57E-02	0.178344		M30	90u/.18u	9.84E-04	5.30E-03	3.71E-01
M31	14.5u/.18u	1.43E-03	5.90E-03	0.484746		M31	191.7u/.18u	9.84E-04	1.26E-02	1.56E-01
Iref	1.3mA	1.3mA				M32	58.3u	9.84E-04	1.18E-02	1.67E-01
						Iref	1.05mA	1.05mA		

VI. Conclusions

The design of a 5th order elliptic switched capacitor filter has been shown using both ideal macro models and real Opamps and Switches. The models can be used to demonstrate many non-ideal effects such as finite opamp gain, finite bandwidth, charge injection, slew rate, and DC offset effects on the overall system transfer characteristics. With real transistor level models, there is a slight drop in the performance, but the filter is still very usable for many applications.

VII. Appendix I: Matlab Simulation Code

```
%%%%  Switched Capacitor Filter Designer
%%%%
%%% Finding the Best Order
[n,Wp] = ellipord(.1,.16,.198,50.5)
[n,Wp] = cheb2ord(.1,.2,.2,50)
[n,Wp] = cheb1ord(.1,.2,.2,50)
[n,Wp] = buttord(.1,.2,.2,50)
%%%% Finding the Best Transfer Function
fs = 100e6;
[num,den]=ellip(5,.16,50.25,2*pi*5.026e6,
'low','s')
H = tf(num,den)
bode(H);
pzmap(H);
[numd,dend] = bilinear(num,den,fs)
Hz = tf(numd, dend, 10e-9)
 %%%% Plotting the output response
hz = fvtool(numd,dend)
format long
 %%% Factor and order biquads
[sos,g] = tf2sos(numd,dend)
gg = g^(1/3);
%%% Find the cofficents for the biquads
(Low Q)
% a0 = (gg*sos(2,3))/(sos(2,6))
% a1 = (gg*(sos(2,2))/(sos(2,6)))
% a2 = (gg*(sos(2,1))/(sos(2,6)))
% b1 = sos(2,5)/sos(2,6)
% b2 = sos(2,4)/sos(2,6)
% K5 = (b1+b2+1)^(1/2)
% K1 = (a0 + a1 + a2)/K5
% K2 = a2 - a0
% K3 = a0
% K4 = K5
% K6 = (b2 -1)
%%% High Q Coefficents
% a0 = gg*sos(3,3)
% a1 = gg*sos(3,2)
% a2 = gg*sos(3,1)
% b1 = sos(3,5)
% b0 = sos(3,6)
% K4 = ((1+b0+b1)^(1/2))*.99
% K5 = ((1+b0+b1)^(1/2))
% K1 = (a0+a1+a2)/K5
% K3 = a2
% K6 = ((1-b0)/K5)*.99
% K2 = (a2-a0)/K5
```

TABLE VI
Opamp Simulated Parameters

Opamp Design Parameter	Simulated Performance
Supply Voltage	1.8
Close Loop Gain	8
Settling Error (static + dynamic)	.604 x 10^{-4}
Load Capacitance (C_L)	2.5 pF
Settling Time	9.95 ns
Peak SNR	73.73 dB
Differential rms Noise Voltage (µV)	.02123 µV
THD (F_{in} = 1 MHz)	-18dB
THD (F_{in} = 24 MHz)	-10dB
Amplifier Core Power Consumption	77.49 mW
Bias Power Consumption (mW)	37.15 mW
Total Power Consumption (mW)	114.64 mW
Differential DC Loop Gain (v_{od}) = 0	105.2 dB
Differential DC Loop Gain (v_{od}) =	78 dB
Differential Loop-Gain Unity gain	131.8 MHz
Differential Loop-Gain phase margin	87.29°
Differential Loop-gain gain margin	-43.21 dB
Common-mode Loop-gain unit gain	6.31 MHz

```
%%%%  Linier Coefficents
% c1 = 10*(sos(1,2)*gg)/abs(sos(1,5))
% c2 = -2*c1
% C3 = (sos(1,4)/abs(sos(1,5)))-1
```

VIII. Appendix II: Opamp Transfer Characteristic Plots

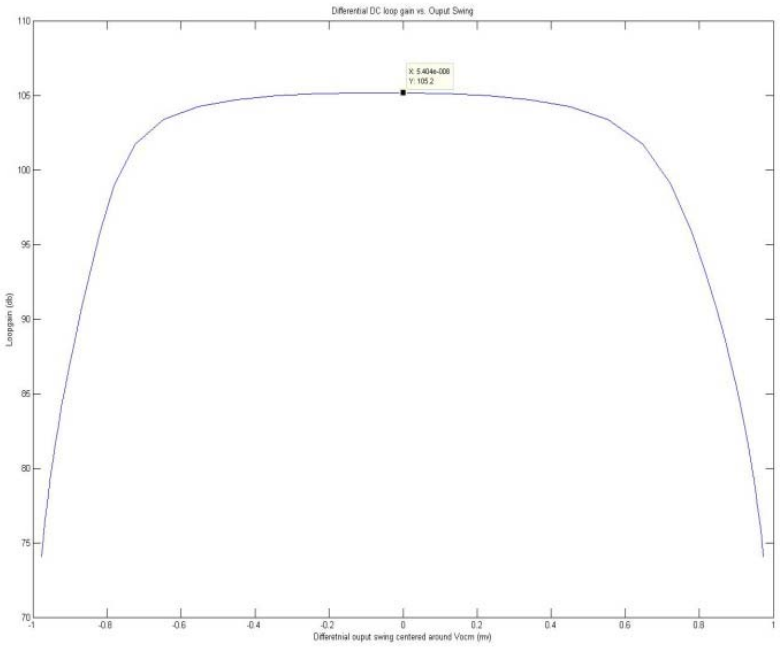

Figure 29: Opamp Output Swing

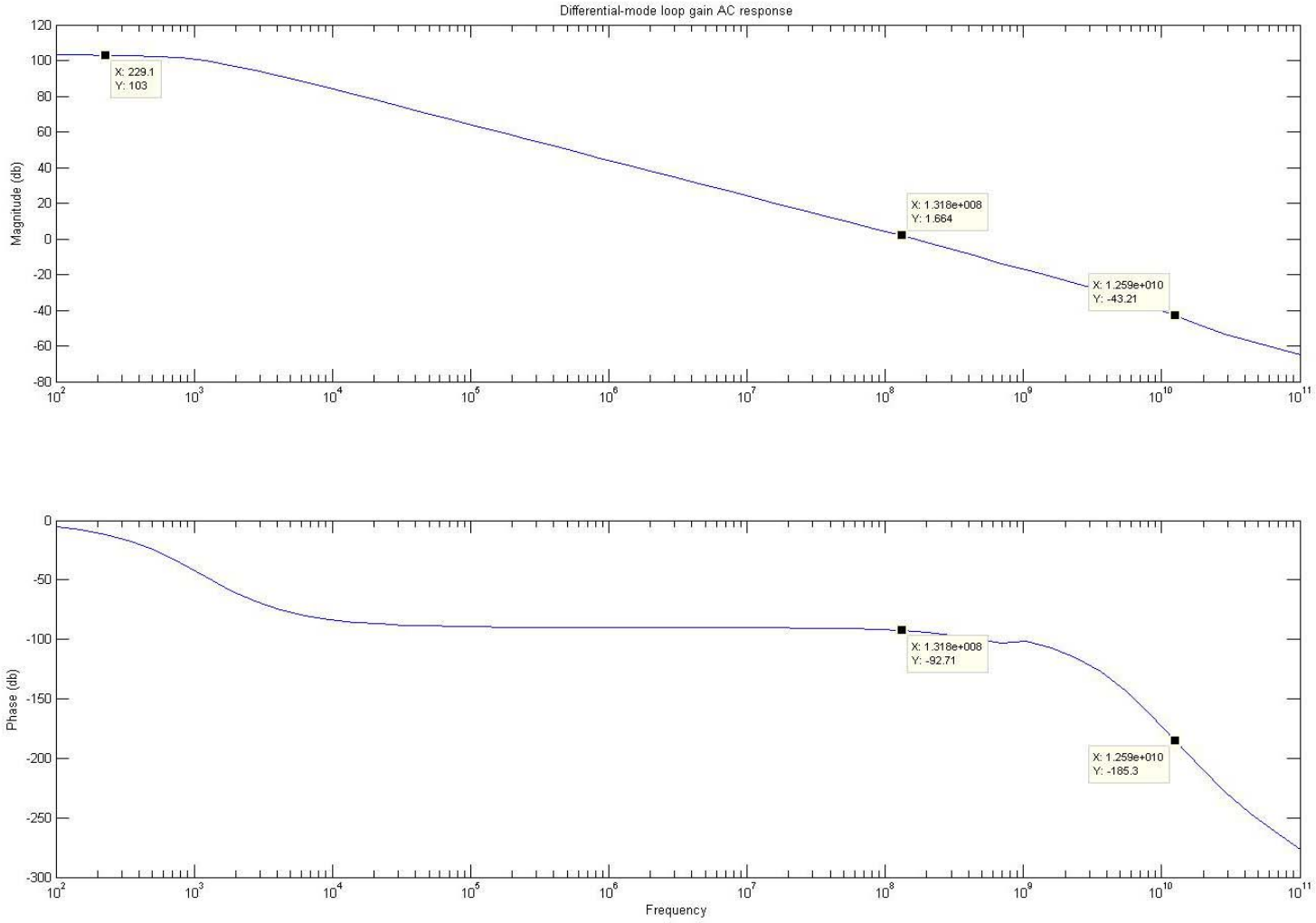

Figure 30: Opamp Closed Loop Magnitude and Phase Response

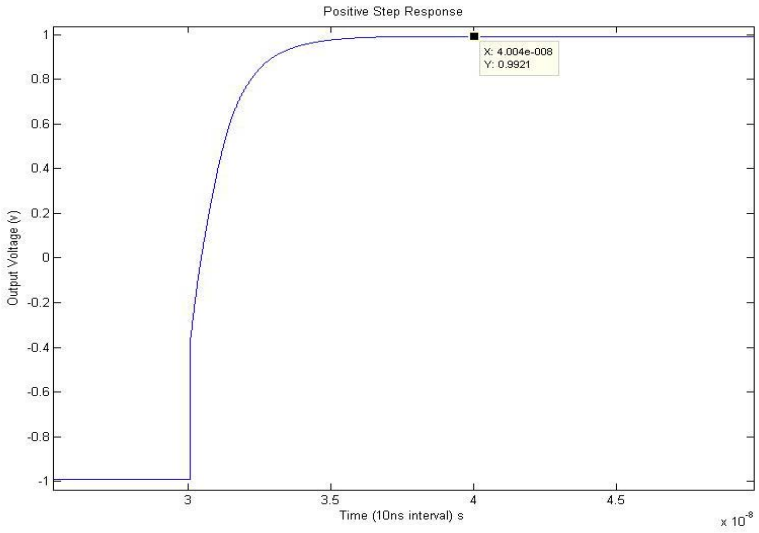

Figure 31: Positive Step Response for a 65mV Input

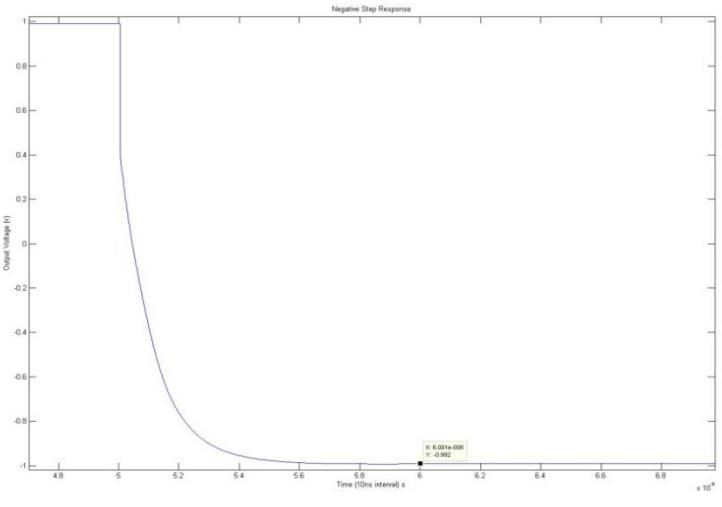

Figure 32: Negative Step Response for a 65mV Input

IX. Appendix III: MATLAB Plotting Scripts

```
%%% Plotting Scripts for Switch Cap
M = csvread('PreDynamic.csv');
P = csvread('PostDynamic.csv');
N = csvread('finite_bw.csv');
S = csvread('Slew.csv');
O = csvread('Offset.csv');
C = csvread('Charge_Inj.csv');
R =
csvread('real_opamp_gain_corrected.csv');

Q = N(:,1)
plot(R(:,1),R(:,2),Q,N(:,2))
axis([0 5e7 -100 10])
xlabel('Frequency(hz)')
ylabel('Magnitude (db)')
title('Filter Frequency Response with
Real Opamps and Simulated Opamps')
legend('Transistor Level Opamps','Ideal
Opamps')

% figure
% J = P(:,1)
%
plot(J,P(:,2),J,P(:,3),J,P(:,4),J,P(:,5),
J,P(:,6))
% xlabel('Frequency(hz)')
% ylabel('Magnitude (db)')
% title('Node Frequency Responses After
Dynamic Range Scaling')
% legend('Opamp 1','Opamp 2','Opamp
3','Opamp 4','Final Ouptut')

% Charge Injection
% plot(C(:,1),C(:,2))
% xlabel('Time (s)')
% ylabel('Magnitude (db)')
% title('Filter Step Response Showing
Slew Rate')
% legend('Step Response')

% Offset Voltage
% V = O(:,1);
%
plot(V,O(:,2),V,O(:,3),V,O(:,4),V,O(:,5),
V,O(:,6),V,O(:,7))
% xlabel('Frequency(hz)')
% ylabel('Magnitude (db)')
% title('Filter Magnitude Response for
Varying Input Offset')
% legend('.0001 V','.001 V','.01 V','.05
V','.1 V','.2 V')

% %Slew Rate
% plot(S(:,1),S(:,2))
% SR = (1.732-.5125)/((1.663e-7)-(9.53e-
8))
% ylabel('Time (s)')
% xlabel('Voltage (V)')
% title('Slew Rate of Filter in Response
to Step Function')
% legend('SR = 17.176 V/us')

% Finite BW
% Q = N(:,1)
%
plot(Q,N(:,2),Q,N(:,3),Q,N(:,4),Q,N(:,5),
Q,N(:,6),Q,N(:,7))
% ylabel('Magnitude (dB)')
% xlabel('Frequency (Hz)')
% title('Finite Opamp Gain on Filter
Frequency Response')
% legend('0 dB','20 dB','40 dB','60
dB','80 dB','100 dB')
% axis([0 5e7 -100 10])
% grid on

% xlabel('Frequency(hz)')
% ylabel('Magnitude (db)')
% title('Node Ouput Voltages After
Dynamic Range Scaling')

% %Normal Output
% plot(Q,N(:,2))
% xlabel('Frequency(hz)')
% ylabel('Magnitude (db)')
% title('Cadence Filter Magnitude
Response')
% axis([0 5e7 -100 10])
% % plot(S(:,1),S(:,2))
```

X. References

[1] D. Johns, K. Martin “Analog Integrated Circuit Design,” John Wiley and Sons Publishing, 1997, NY,NY.

[2] R. Schumann, M. Van Valkenburg “Design of Analog Filters,” Oxford University Press, January 2001.

[3] Dr. Gabor Temes Lecture Notes.

XI. Author

Jon Guerber (S’05) received the B.S. degree in Electrical Engineering from Oregon State University in 2008 and is currently working towards a Masters in Electrical Engineering from Oregon State University.

During the Summer of 2008 he was with Teradyne Corp developing high frequency signal tracking and active power management solutions for semiconductor test devices. During the 2007 he was with Intel Corp. investigating high performance, small form factor motherboard architectures to support future PC microprocessor requirements. He is currently a research member of the Analog and Mixed Signal group at Oregon State University in Corvallis, Oregon with a focus in the area of deep-submicron, low-voltage Analog to Digital Conversion.

Mr. Guerber is a life member of the Eta Kappa Nu Electrical Engineering Society and an Active Wikipedia Electronics Contributor.