

# Design of an 2.4 GHz CMOS Low Noise Amplifier

Jon Guerber ECE 621, Winter 2010

**Abstract**— The design and simulation of an inductively degenerated CMOS Low Noise Amplifier (LNA) is presented operating at 2.4 GHz. The LNA has a noise factor less than 2dB and a forward gain greater than 18dB with actual chip parasitics and gate noise modeled. This design was completed in .18u technology with a 1v supply. The input and output power matches are better than -12 dB.

## I. INTRODUCTION

Wireless mobile devices have permeated our modern society allowing us to communicate in nearly any location, gather data from the deep reaches of space, and locate ourselves on this ever smaller planet. However, unlike digital electronics, the analog circuitry used to make wireless communications possible has not benefited from the intense device scaling to the same degree. Current wireless designs still face noise, matching and signal detection challenges.

Perhaps the most crucial block in the wireless design flow in the low noise amplifier. This block has the job of matching the antenna input with the rest of the circuitry and simultaneously amplifying it for further processing (See Figure 1). Noise is critical in this block since the input is extremely weak and can be easily corrupted by even small amounts of thermal noise.

This work will investigate the tradeoffs needed to design a Low Noise Amplifier in modern CMOS processes with reduced supply voltages that are compatible with digital processes. The design will be done in four steps. The first is the ideal design, followed by an analysis of the on-chip inductors. Finally, the design will include bond wire parasitics and the possibility of low inductance packaging. Simulations will be conducted using Advanced Design System (ADS).

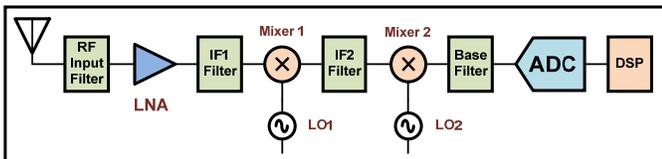


Figure 1: RF Receiver Block Diagram

## II. LNA DESIGN WITH IDEAL INDUCTORS (PART A,B)

The design requirements for the Low Noise Amplifier are given in Table 1. The basic design of an LNA is an inductively degenerated cascode common source amplifier. This configuration provides reasonably high gain with input matching provided by the inductive source degeneration. The simulated design with no inductor parasitics is shown in figure 2.

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TABLE I  
LOW NOISE AMPLIFIER DESIGN REQUIREMENTS

Parameter	Specified Value
Supply Voltage	1v
Operating Frequency	2.4 GHz
Noise Figure	< 2 dB
Power Consumption	<1mW
S11	< -12 dB
S21	> 12 dB
S12	<-15 dB
S22	<-12 dB

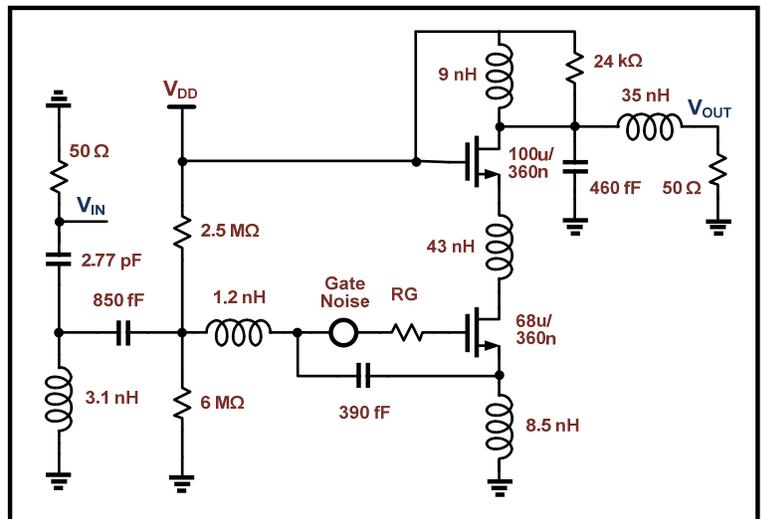


Figure 2: LNA Circuit Design with Ideal Inductors

Sizing the active transistors in the circuit requires parallel thought about the circuit noise. Mosfet lengths have been chosen to be .36u ( $2 * L_{min}$ ) to provide lower gate and drain noise (allowing  $\gamma = 2/3$  and  $\delta = 4/3$  as in long channel models). The width of the main transistor was chosen based on the power constrained noise optimization outlined in [1]. Modeling the impact of noise from the distributed gate resistance is vital and is modeled using the following equation from [2] where  $g_{d0}$  was modeled in a separate simulation:

$$\overline{v_g^2} = 4kT \delta r_g \quad \text{where} \quad r_g = \frac{1}{5g_{d0}}$$

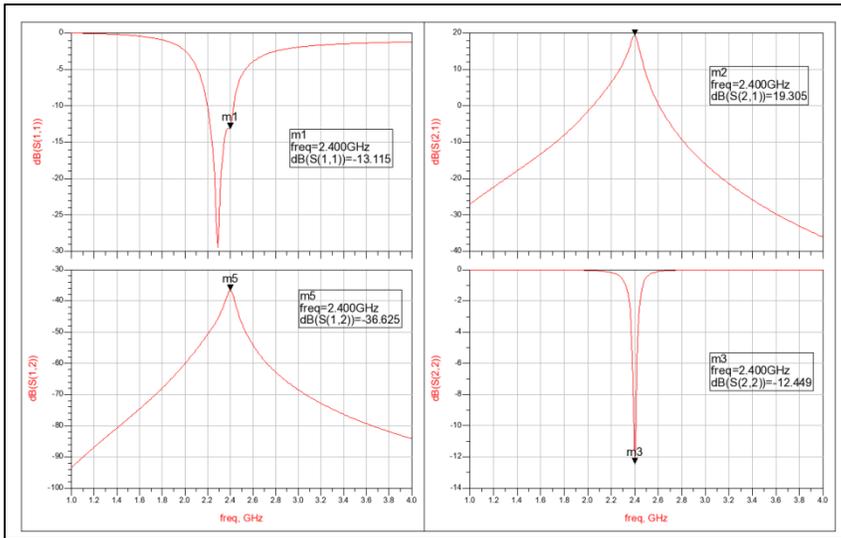


Figure 3: LNA S-Parameters with Ideal Inductors

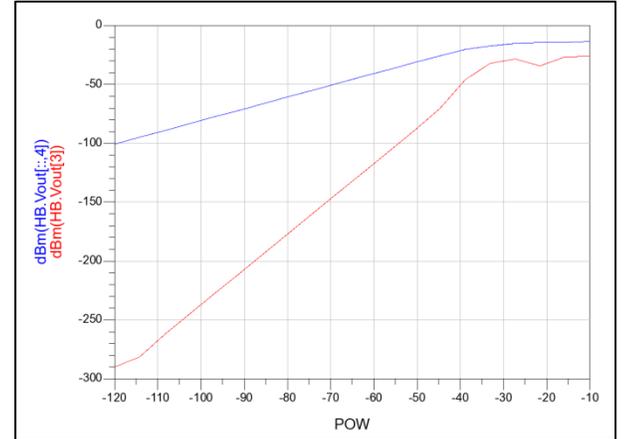


Figure 5: LNA IIP3 Plot with Ideal Inductors

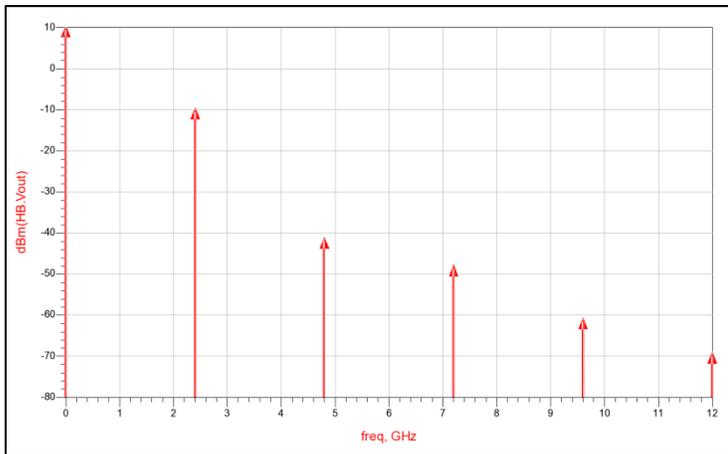


Figure 4: LNA Frequency Response with Ideal Inductors (-12 dBm Input)

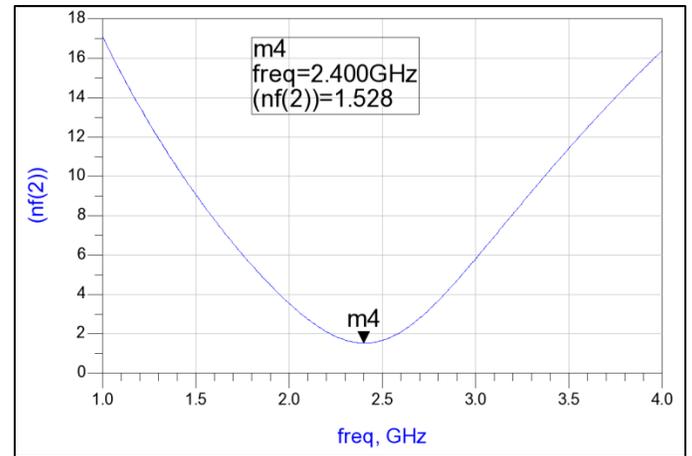


Figure 6: LNA Noise Figure with Ideal Inductors

The size of the inductive degeneration and gate inductance were initially determined to optimize the input match (with  $L_s$ ) and resonant frequency ( $L_g$ ). By adding an input matching network as was shown in [3] and canceling the capacitance at the cascode node with another inductor, it is possible to relax the source inductance matching and gain considerations. The source inductance was then adjusted in tandem with the source external capacitance to optimize noise performance. While larger than normal, the chosen source inductance proved to be the best match for the design requirements.

Following the design of the input network, the cascode output was chosen to provide a high impedance at the resonant frequency. A simple downward transformer matching network was then employed to allow the termination to see 50 ohm impedance. A physical resistor with very loose accuracy requirements was also added at the output of the cascode node to improve the match from the termination looking in.

With the majority of the parameters set, the width of the cascode transistor was tuned to provide optimal forward gain without adding excessive noise. Finally, stage biasing is provided by a resistor ratio, but can be replaced with a current mirror if needed.

Shown in Figure 3, are the S-Parameter results from the LNA with ideal inductors and specifications are met with noise included. Figure 4 shows the frequency response for a -12 dBm input. Notice that the fundamental at the output is much below zero due to the non-linearity that occurs at powers above about -20 dBm. While not a design criteria, large signal linearity would be important in many applications.

The IIP3 of the simulated circuit was -21.4 dBm and the fundamental and third harmonic powers are shown in Figure 5. While not a superb IIP3, inter-modulation linearity was not a design goal for this project. The noise figure of the circuit is shown in Figure 6 and is much lower than the requirement of 2dB. This was due to the careful choosing of device sizes and auxiliary inductance sizes.

### III. LNA DESIGN WITH ON-CHIP SPIRALS (PART C,D)

The next step in an increasingly realistic LNA is to create the on-chip spirals and include their respective parasitic elements. The two small inductors that had to be made on-chip were the input match inductor and the gate inductor as seen in Figure 7.

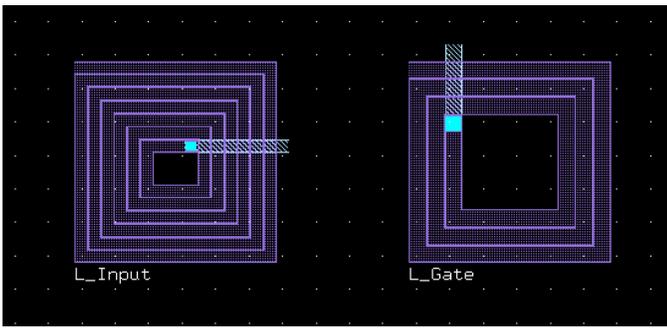


Figure 7: On-Chip Spiral Inductors Designed with ASITIC

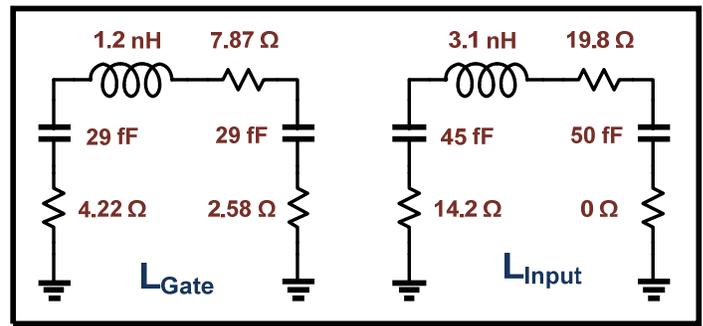


Figure 8: On-Chip Spiral Inductors Parasitic Modeling

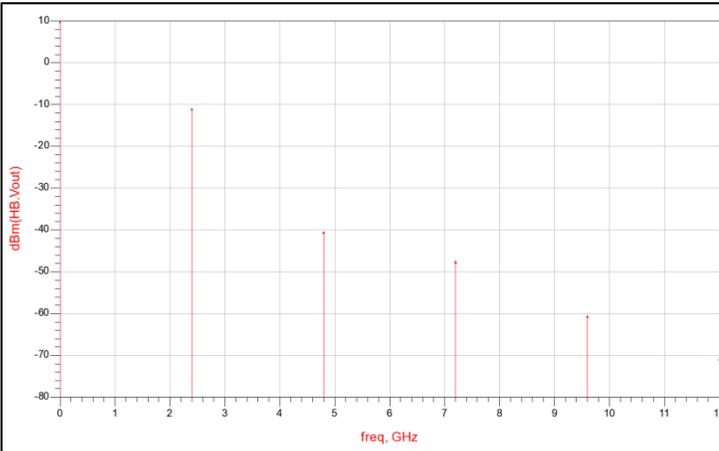


Figure 9: Frequency Response with Package Pin Parasitics (Part E)

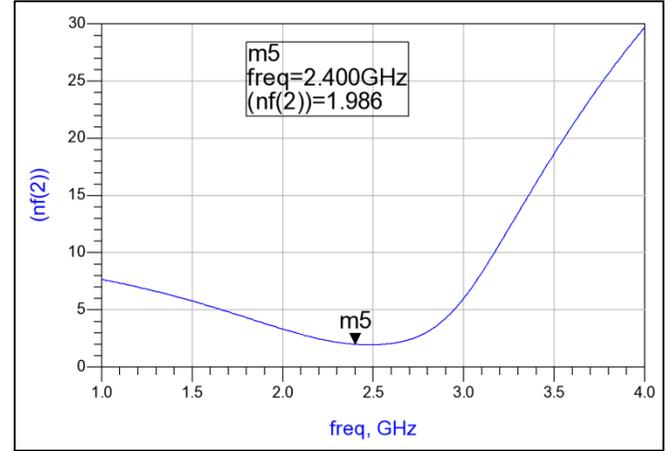


Figure 10: Noise Figure with Package Pin Parasitics (Part E)

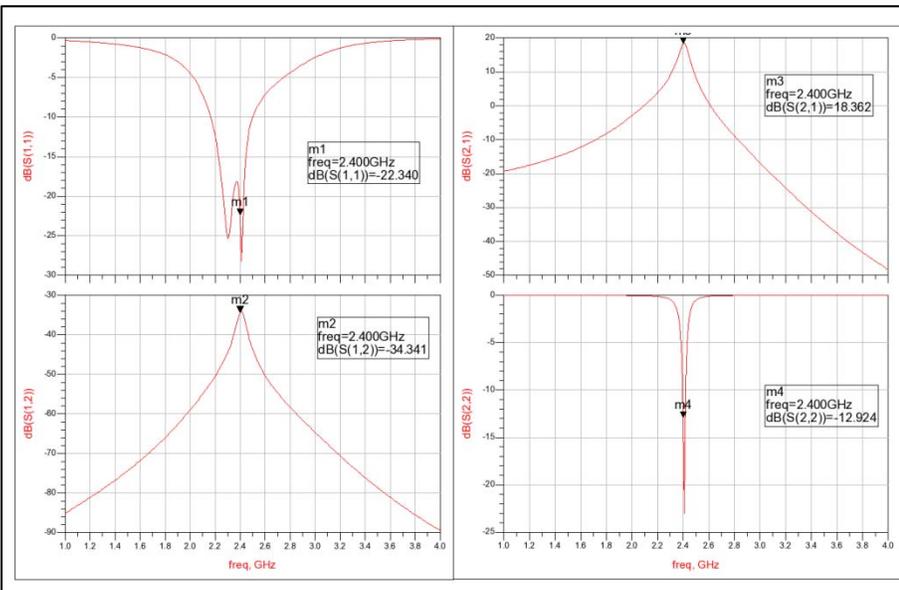


Figure 11: S-Parameters with Package Pin Parasitics (Part E)

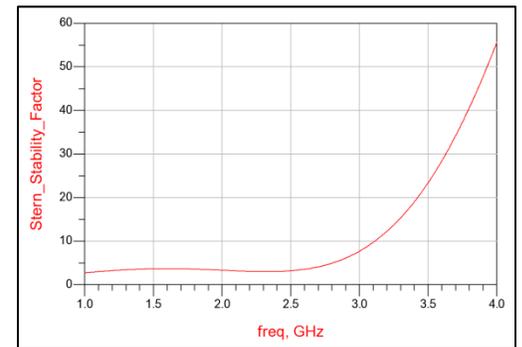


Figure 12: Stern Stability Factor (Part E)

With the additional of these parasitic inductors the LNA noise figure increased to about 4.3 dB with all other parameters matching. This is mostly due to the large parasitic elements on the input matching inductor shown in Figure 8. The Q of both inductors was optimized by using the ASITIC “OptSq” function and was about 2.2 for both.

Further details for the simulation with just the on-chip coils can be found in the performance summary.

#### IV. LNA DESIGN WITH PIN PARASITICS (PART E,F,G)

While the small inductors were implemented on-chip, larger inductance values were achieved with bondwires and external components. For every bondwire pad, there is an accompanying capacitance that has been added. In addition, input inductance was added to account to pin to antenna traces and wires. Simulated results with these parasitics can be found in Figures 9-12.

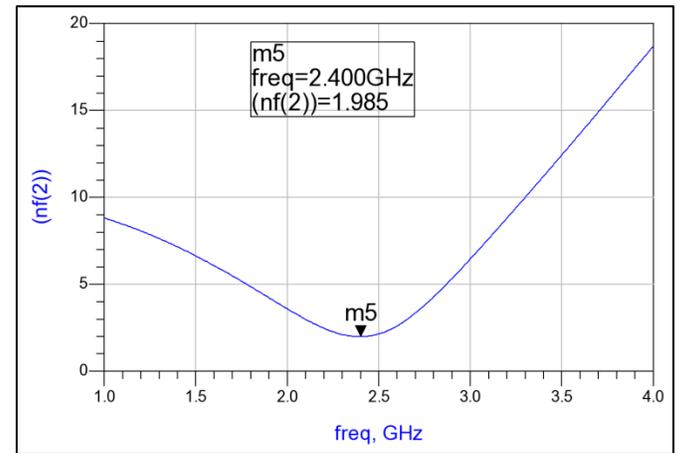
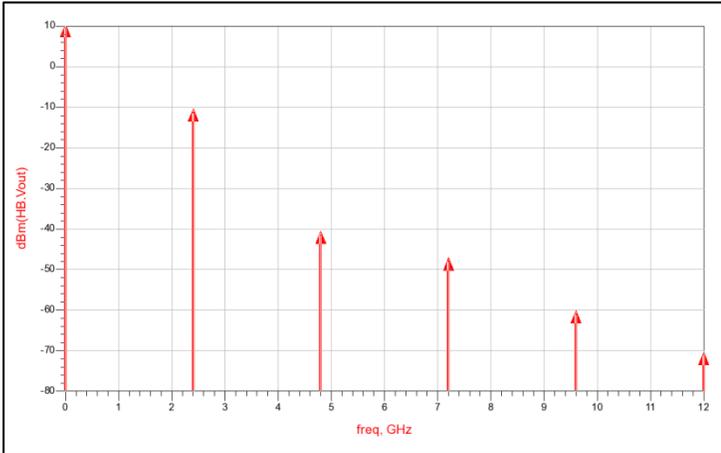


Figure 13: Frequency Response with Reduced Package Pin Parasitics (Part F)

Figure 14: Noise Figure with Reduced Package Pin Parasitics (Part F)

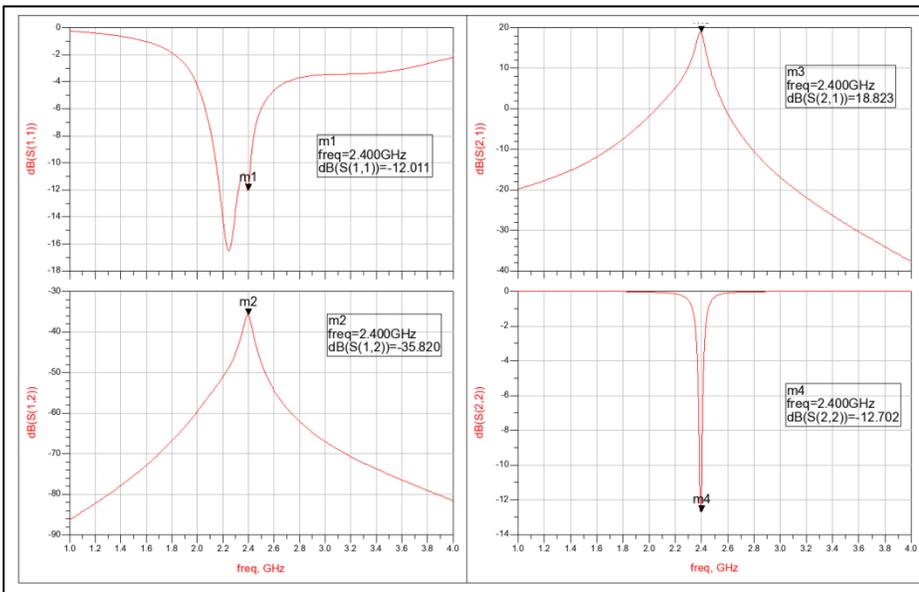


Figure 15: S-Parameters with Reduced Package Pin Parasitics (Part F)

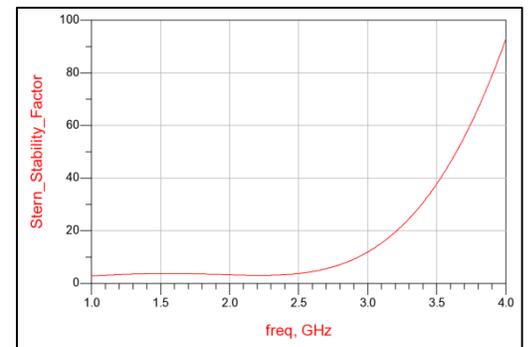


Figure 16: Stern Stability Factor (Part F)

With the inclusion of package pin parasitics, there were many design changes that had to be made. The input network providing matching is now greatly disturbed by the package bondwire input inductance. To account for this, the input network is changed and the previously designed on-chip input spiral is removed. Following these adjustments, the noise figure (Figure 10) is still much higher than in the ideal case.

Figure 12 shows the stern stability factor which is around 4 at 2.4 GHz which was calculated with the following equation:

$$K = \frac{1 + |s_{11}s_{22} - s_{12}s_{21}|^2 - |s_{11}|^2 - |s_{22}|^2}{2|s_{21}||s_{12}|}$$

A factor greater than 1 means the system is unconditionally stable. The simulated IIP3 is -17.61 dBm.

With the reduction of the bondwire inductance from 6 nH to 2 nH, matching and parasitic issues become much more manageable. One possible problem is that the reliance purely on bondwire inductance is now more difficult, however, since we are using bondwires with external inductors, there is no problem. Figures 13-16 show the LNA performance with 2 nH bondwire inductance.

The FOM of the LNA calculated with the following equation which compares noise, gain and linearity [4]:

$$FOM = 10 \log \left[ 100 \left( \frac{|s_{21}|(dB)}{(F-1)P_{dc}(mW)} \right) \left( \frac{OIP3(mW)}{P_{dc}(mW)} \right) \right]$$

The FOM is 30.22 with 6 nH bondwires and 28.23 with 2 nH bondwires. This would have been state of the art in about the year 2001.

TABLE IV  
LNA PERFORMANCE SUMMARY

Parameter	Ideal Inductors	On-Chip Inductors	On-Chip and Bondwire Inductors (6nH)	On-Chip and Bondwire Inductors (2nH)
Noise Figure (dB)	1.528	4.262	1.986	1.985
S11 (dB)	-13.115	-12.21	-22.34	-12.011
S12 (dB)	-36.625	-39.31	-34.34	-35.82
S21 (dB)	19.305	16.64	18.362	18.823
S22 (dB)	-12.449	-12.995	-12.924	-12.702
IIP3 (dBm)	-21.4	-20.8	-17.61	-18.38
Stern Stability Factor	NA	NA	4	4
FOM	NA	NA	30.22	28.23

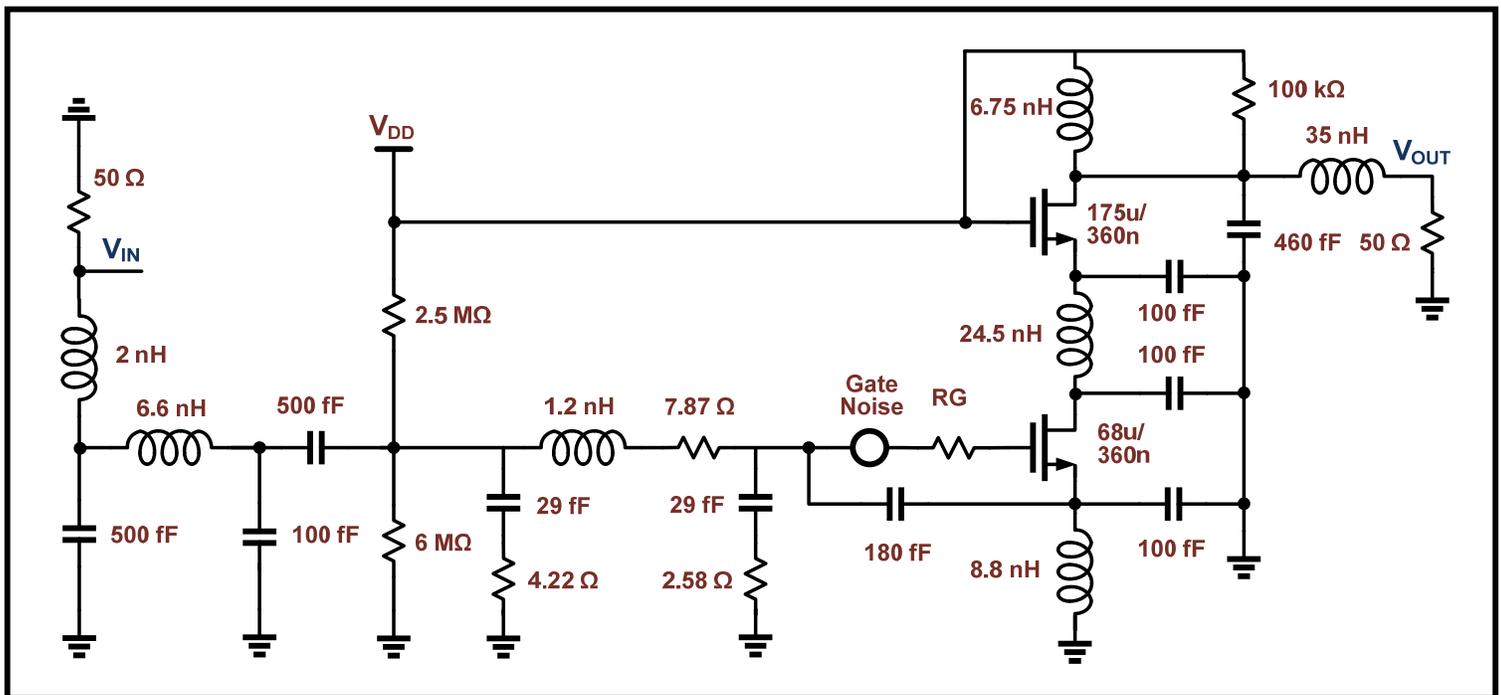


Figure 17: Final LNA Schematic Including On-Chip Inductors and BondPad Capacitances (Some Bondpad Caps Have Been Lumped With Existing Capacitors)

## V. LNA CONCLUSIONS

This paper has presented the design of a sub 2dB Noise figure CMOS LNA. A lesson learned in this design is the importance of intuitive understanding of resonance and circuit theory when designing LNAs. Pre-calculations just cannot be complete enough to fully model the circuit and some adjustments are necessary.

## VI. REFERENCES

- [1] T. Lee, "The Design of Radio Frequency Integrated Circuits," Second Edition, Cambridge, 1998.
- [2] D. Shaeffer and T. Lee, "A 1.5-V 1.5-GHz CMOS Low Noise Amplifier," JSSC, May 1997.
- [3] T. Nguyen, et. al., "CMOS Low Noise Amplifier Design Optimization Techniques," IEEE Transactions on Microwave Theory and Techniques, May, 2004.
- [4] G. Gramegna, "A Sub-1-dB NF 2.3kV ESD-Protected 900-MHz CMOS LNA," JSSC, July 2001.

## VII. AUTHOR



**Jon Guerber** (S'05) received the B.S. degree in Electrical Engineering from Oregon State University in 2008 and is currently working towards a Masters in Electrical Engineering from Oregon State University.

During the Summer of 2008 he was with Teradyne Corp developing high frequency signal tracking and active power management solutions for semiconductor test devices. During the 2007 he was with Intel Corp. investigating high performance, small form factor motherboard architectures to support future PC microprocessor requirements. He is currently a research member of the Analog and Mixed Signal group at Oregon State University in Corvallis, Oregon with a focus in the areas of deep-submicron, low-voltage Analog to Digital Conversion and continuous time filters.

Mr. Guerber is a life member of the Eta Kappa Nu Electrical Engineering Society and an Active Wikipedia Electronics Contributor.