Design and Analysis of a Self Biased Flicker Noise Cancelling CMOS Direct Conversion Mixer

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***Abstract*— The design of a double balanced CMOS downconversion mixer is presented with a novel calibration scheme for pulse injection flicker noise reduction. This self-biasing calibration technique enables the reduction of the mixers' noise figure by over 20dB at baseband frequencies without any additional reference voltages, manual adjustment, or large inductors. This results in simpler IC testing and manufacturing as well as reduced design cost (for an accurate voltage reference). The design is simulated in 90nm CMOS with Verilog-A digital models. In addition, the source and manifestation of flicker noise in mixer parameters is analyzed.**

I. Introduction

Wireless communications has become a common feature of our everyday life. From the ordinary consumer talking on a cellphone to nations developing cross planet communication mechanisms, the demand for wireless connectivity has never been greater. However, our current wireless spectrum is currently saturated with nearly all avalible bandwidth being occupied and free portions selling for millions of dollars. In addition, consumers are demanding products that function with ever shrinking form factors and use lower power. One of the potential solutions to these problems is the direct conversion receiver architecture.

The direct conversion architecture allows for reduced backend data conversion bandwidth (lower power), and reduced filtering requirements. To allow direct conversion receivers to function with small RF signal bandwidths, the downconveriosn mixer must bring the output signal to very low frequencies close to the baseband. Traditionally this has faced many problems with frequency drift and offset, however many solutions for these problems have been proposed and tested. One problem that still plagues direct conversion receivers though is the presence of flicker noise in the baseband with power levels high enough to corrupt the signal of interest. This paper will discuss why this flicker noise occurs and how to reduce the unwanted noise at the output of a double balanced mixer.

Section two of this paper will discuss the mechanisms of how flicker noise arrives at the baseband output of a mixer. Section three will then examine some approaches that have been shown to reduce the impact of this noise and discuss their limitations. Section four will outline the method to determine the optimal bias voltage. Section five will present the proposed self biasing mixer structure and outline the implementation of the design. Section six will then present simulation results followed by system conclusions in section seven.

As a note, this project was simulated in 90nm CMOS with a 1.2v supply rail. The process change from the class process was both to see small dimension effects and fully utilize transient noise simulations available for the process.

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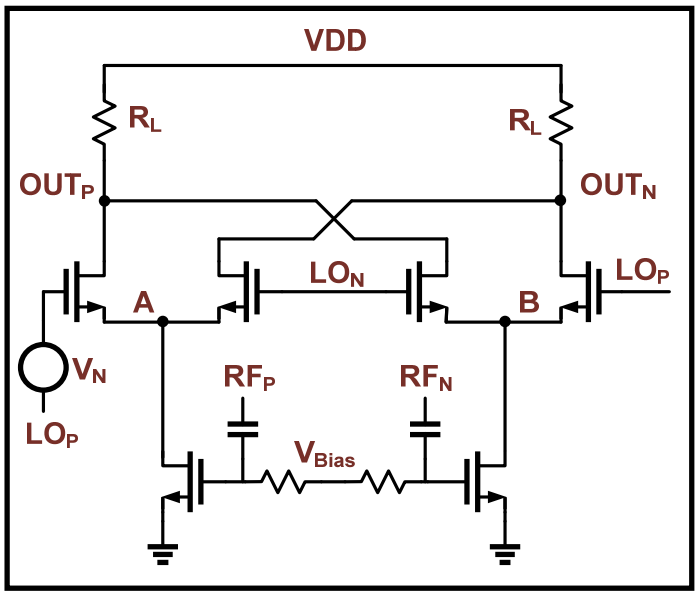

Figure 1: Standard Double-Balanced Gilbert Mixer with Input Referred Switch Noise

II. Flicker Noise Generation

Downcoversion mixers are crucial in receiver structures since they translate an RF signal down to the baseband where it can be digitized. Any noise at the RF signal frequency will also be translated. Ideally, any noise component of the RF signal that is at the baseband frequency will not appear at the output of the mixer but rather be translated to a higher frequency by the switching of the Local Oscillator (LO). However, in fabricated receivers, it can be show that there is a significant flicker noise contribution at low frequencies that can corrupt a mixed signal.

While the physical generation of flicker noise is not fully understood, observations have been made about the generation of this noise that can aid in the circuit design process. According to [1], flicker noise can be generated from two main methods, the direct and indirect.

The direct method of flicker noise generation comes from the referral of the flicker noise current to the voltage input at the gate of the switching transistors (Figure 1). Ideally, the current output of a mixer should take the trasncoductor current and simply switch it from one side to the other. With an input referred flicker noise, there is now some imbalance in this switching which can be pictured as injected noise pulses as shown in figure 2 [1]. This injection allows low frequency flicker noise originating from the transconductors or switches to move directly to the output. The flicker noise injection is directly related to the slope of the LO at the switching frequency since an infinite sloped LO will not cause the zero crossing points of the switch inputs to change and no imbalance will be seen.

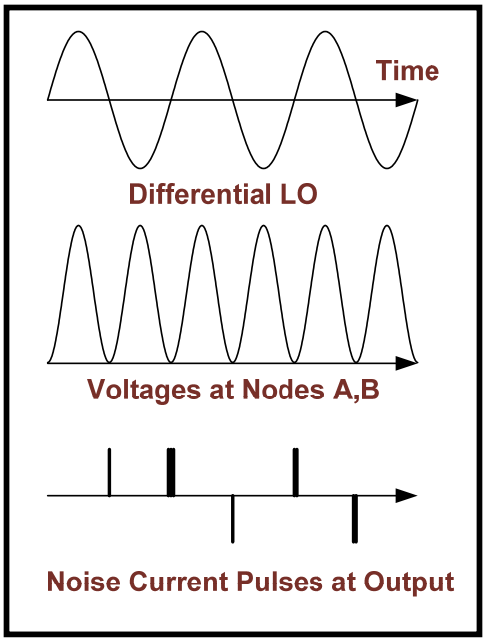

Figure 2: Mixer Node Waveforms and Flicker Noise Induced Current Pulses

Direct flicker noise current pulses have been shown in [1] to be modeled to a first order by the following relation:

$$i_{NP} = \left(\frac{2}{T}\right)(2I)\left(\frac{V_N}{S}\right) = 4I\frac{V_N}{ST} \qquad (1)$$

Where T is the period of the LO, S is the slope at the switching instant, I is the amplitude of the commuted current, and Vn is the input referred switch flicker noise. Thus to decrease the impact of switch flicker noise we should either reduce the LO frequency, increase the slope of the LO, or reduce the switch current.

The second source of flicker noise feedthough to the output is from what is known as the indirect method [1]. This method assumes that the slope of the LO is infinite, but there is parasitic capacitance on the nodes A and B of the mixer. Due to the input flicker noise voltage of the switches, there is a finite difference in the voltage on nodes A and B with each switching operation. The switching of the mixer will cause a current to flow from the parasitic capacitance at the instant of switching which will cause similar noise pulses to appear at the output as from the direct generation method. The indirect noise current can be modeled to a first order by the following:

$$i_{nI} = \left(\frac{2}{T}\right)C_P V_N \qquad (2)$$

Where Cp is the parasitic capacitance on the nodes A and B and Vn is the switch input referred flicker noise.

One aspect of flicker noise that we still have not investigated is why the switches have flicker noise in the first place. Flicker noise is present in all MOS devices due to traps in the channel region. It can be shown in [2] that flicker noise is proportional to the input current and inversely proportional to device capacitance.

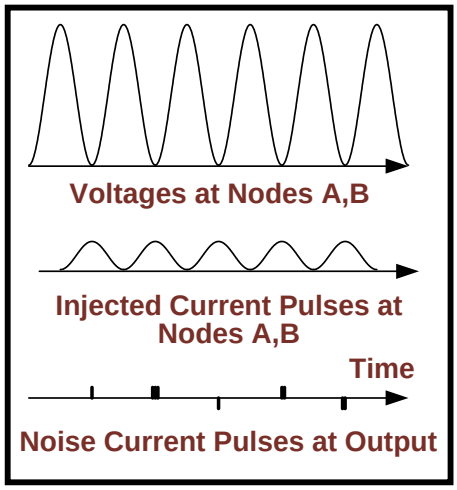

Figure 3: Mixer Switching Node Voltage, Injected Current and Reduced Flicker Noise Pulses

Mean square flicker noise current is approximately given by the following [2]:

$$\overline{i_n^2} = \left(\frac{K}{f}\right)\left(\frac{g_m^2}{WLC_{OX}^2}\right)\Delta f \approx \left(\frac{K}{f}\right)\mu_N(2)\left(\frac{I_D}{L^2}\right)\Delta f \qquad (3)$$

Where K is a device constant. The approximation on the right assumes a long channel device. While this may not always be absolutely accurate, the dependence on the bias current is still present.

III. Flicker Noise Reduction Techniques

The problems of flicker noise in direct conversion receivers is sufficiently sever to enable a good amount of research into how to combat it. The basic methodology involves examining the flicker noise mechanisms and seeing what parameters can be controlled. Output flicker noise is a function of the LO slope, operating frequency, device size, material properties, and device current. Of these parameters, only the device current can be easily controlled for a given mixer.

One of the first methods to improve the output flicker noise is to inject a constant bias current into nodes A and B in figure 1. This will reduce the current flowing though the switches while maintaining the transconductance of the input stage. While it has been shown in [3] to be helpful, this technique can never completely eliminate flicker noise, increases the input resistance of the switches, increases power consumption, and can be shown to reduce mixer linearity [4]. The authors of [3] have attempted to improve this current bleeding performance with limited success.

A second flicker noise reduction technique and the one that will be leveraged for this papers proposed technique is the current injection scheme. One observation is that flicker noise will only flow to the output during times where the zero crossing point of the switches is mismatched. Thus by making the switch current go to zero at the switching instant, flicker noise will not be transmitted to the output. It's important to note that this will not eliminate flicker noise production, but rather just its transmission to the baseband output. To make the switch current go to zero, one can inject current pulses at the switching instant as shown in figure 3. This will reduce the current noise pulses ideally to zero and eliminate input to output flicker noise transmission.

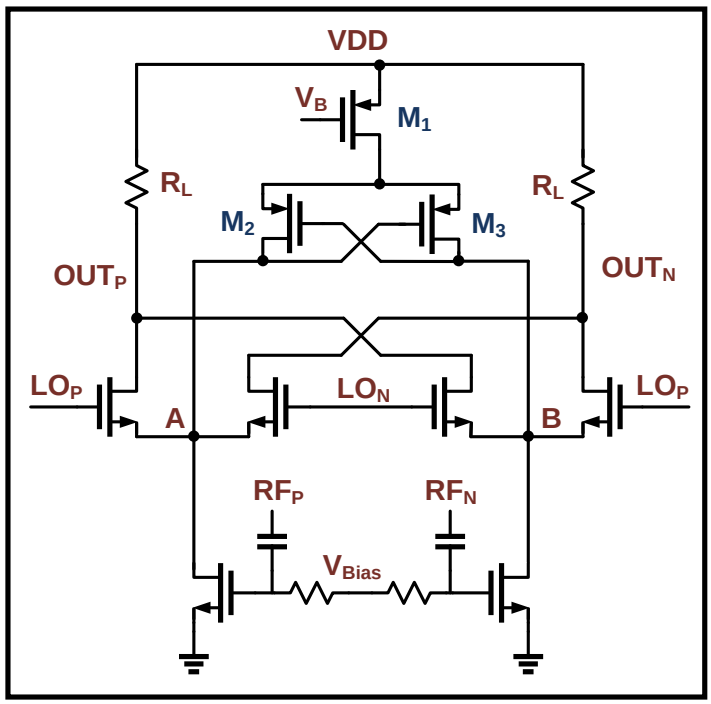

Figure 4: Double Balanced Mixer with Dynamic Current Pulse Injection

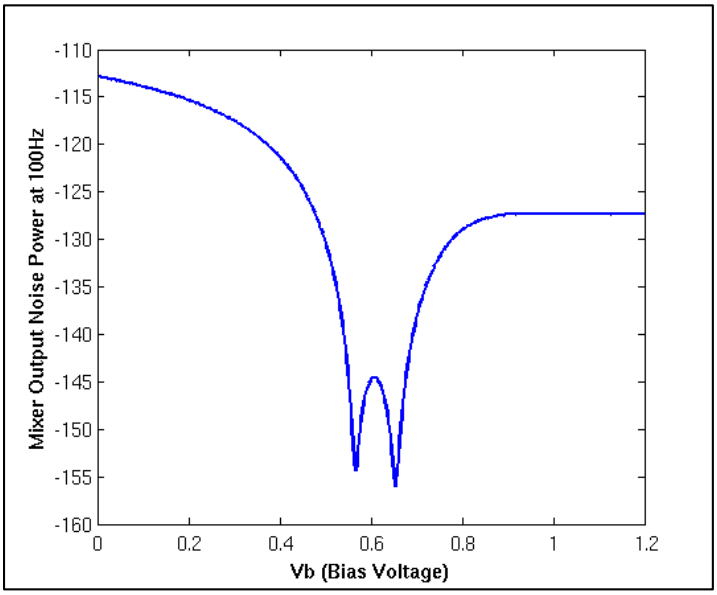

Figure 5: Flicker Noise Power at 100Hz for a Given Vb

To implement the current injection scheme, the authors of [4] have implemented the circuit shown in figure 4. In this implementation the transistor M1 sets a current that can be triggered on when the voltage to M2,3 gets to a low enough value. The switches should be sized so that a reasonable bias voltage will eliminate the current though the switching transistor during each LO transition. This scheme works well and has been shown to remove nearly all flicker noise from a mixer.

The one hitch that makes this system impractical for product development is the current injection bias voltage Vb. Vb will set the amount of current delivered to the switches during a transition if it is incorrect, flicker noise will travel to the output of the mixer. As shown in figure 5, output flicker noise is a sensitive function of Vb. If this design were to be made into a manufactureable product, a very accurate and temperature intolerant reference voltage would have to be generated using power, area and design time. Furthermore, each fabricated mixer should be individually tuned to provide the correct noise rejection increasing the time to market and ultimately costing the manufacturer money. This project is thus to determine a method of finding the optimal Vb and calibrate the mixer to this value automatically.

IV. Proposed Flicker Noise Cancelling Vb Determination

In order to determine the correct bias voltage Vb to eliminate flicker noise, we must understand the conditions that cause the current in the switching transistors to go to zero. Generally, using figure 4 as a reference, during a transition, the effective impedance looking up at the switches increases due to the switch Vgs lowering. This causes the voltages at node A and B to be small when the mixer is switching from one side to the other. Using a similar argument, the output nodes will also increase in voltage at the switching instant since the switch impedance grows. Notice that this occurs twice per LO period, which is what causes the large spur at 2*LO Hz in double balanced mixers.

Using figure 6 as a model of the components connected to nodes A and B in figure 4, we can derive an approximate formula for the voltage at the node A when switching. From KCL, we have the following formula for the minimum flicker noise point (Is = 0):

$$I_J = I_T - I_{CS} \qquad (4)$$

By assuming that the voltage at node A falls as a ramp, we can approximate the current though the capacitor (Ics) as the following [5]:

$$I_{CS} \approx C\left(V_{MIN}\right)\left[\frac{t}{\tau}\left(e^{\frac{-RT+t}{\tau}}\right)\left(1-e^{t/\tau}\right)\right] \qquad (5)$$

Where tao is the RC time constant, Vmin is the lowest ramp voltage, RT is the rise time (fall time here) and t is the current time. The current though the transconductor and current injector can be crudely approximated as follows:

$$I_J \approx \frac{\alpha}{V(t)} \qquad I_T \approx \beta\left(1+\lambda V(t)\right) \qquad (6)$$

Where alpha is a constant (in reality it should be non-linear) and beta are device parameters of the transconductor. By combining the equations, we can find the following relation for when Is = 0:

$$\left(\beta\lambda\right)V(t)^2 - \left[\frac{t}{\tau}e^{\frac{-RT+\tau}{\tau}}\left(1-e^{t/\tau}\right)+\beta\right]V(t)-\alpha \approx 0 \qquad (7)$$

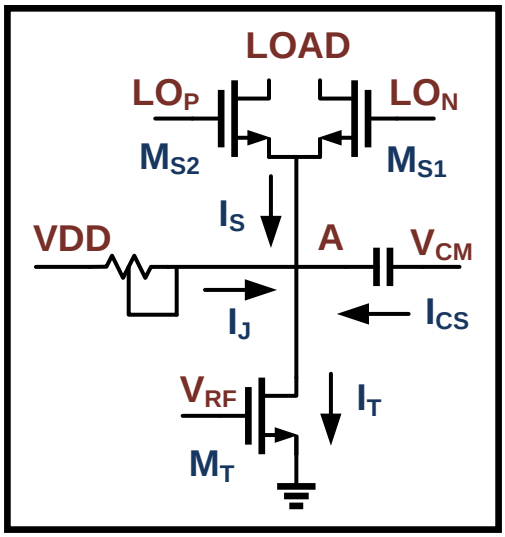

Figure 6: Model for Currents at Node A During Switching Instant

There are two points to the derivation shown in equations 5-7. The first is that there are two real positive roots for when the current though the switch is zero. This is why the plot in figure 5 shows two minima for the flicker noise. The other observation is that figuring out the exact time these minima occur is extremely tough and dependent of many unmeasurable parameters (not to mention that equation 7 is a first order approximation of the real circuit!).

While the prospects for calibrating this mixer circuit might seem bleak, an interesting discovery was made during the course of the project. It was empirically found (though much painful analysis and simulation) that the current though the switching transistors at the switching moment is closely related to the Vds of the transistor at the same switching moment. It was further found that by choosing device sizes correctly, the Vds of the switching transistor can be maximized at the moment the current is zero. It was even further found that this optimized point is not very sensitive to temperature and process mismatch. Thus the mixer can be sized to reliably minimize flicker noise when the switching transistor's Vds is maximized at the switching instant. The optimal value of Vb for this mixer is then that which make Vds maximum at the switching instant.

V. Proposed Flicker Noise Calibration Implementation

To find the optimal Vb, it is now clear that we must sweep Vb until we find the Vds max of the switching transistors (at the switching instant). While this can be challenging to do with just analog components, this problem becomes simpler in the digital domain. Thus the outline of the proposed calibration method is to digitize the value of the switching transistor Vds at the switching instant, then pass it though a digital calibration block which will generate UP and DOWN signal for a charge pump. After a certain amount of time, the optimal Vb will be generated at the output of the charge pump that corresponds to the maximum switching transistor Vds (See figure 7).

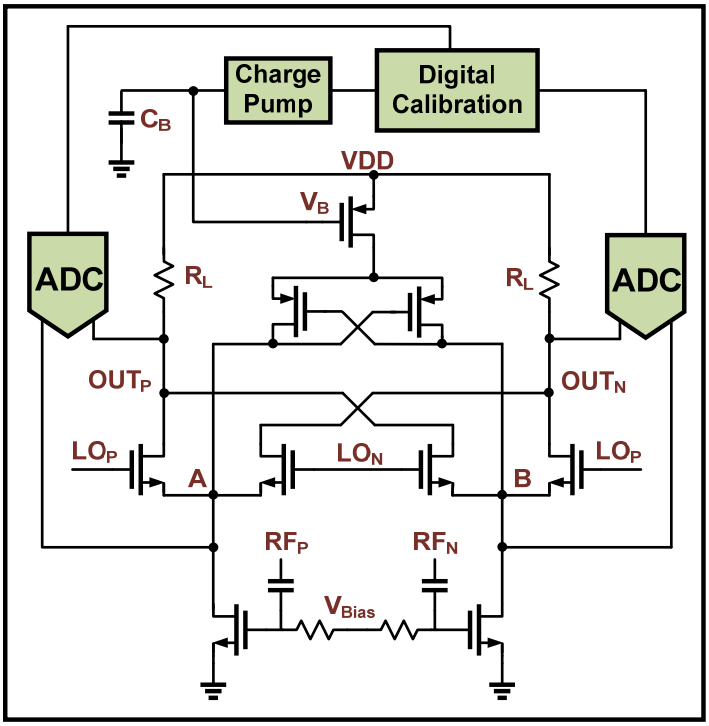

Figure 7: Proposed Mixer Flicker Noise Calibration Block Diagram

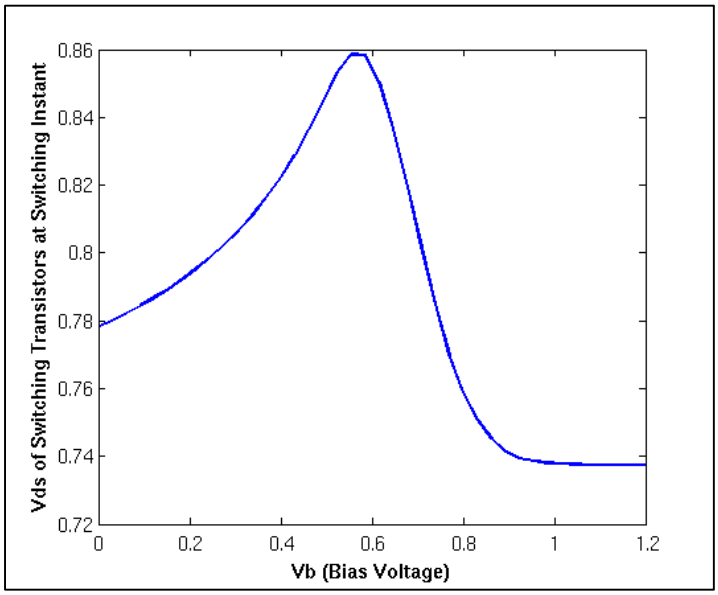

Figure 8: Variation of the Vds of the Switching Transistors vs. Vb

In order to design the calibration block, it's important to note that the maximum Vds of the switching transistors at the switching instant is ideally an increasing function to the peak value (see figure 8). This means that a calibration scheme that implements a peak finding application is to be used. Due to process and supply variations, it would be useful to run this calibration in the background while the mixer is operating. It has been found that by sampling both sides of the mixer and averaging in the calibration block, as shown in figure 7, provides a more accurate Vb estimate when the RF input signal becomes large and some non-linear effects appear.

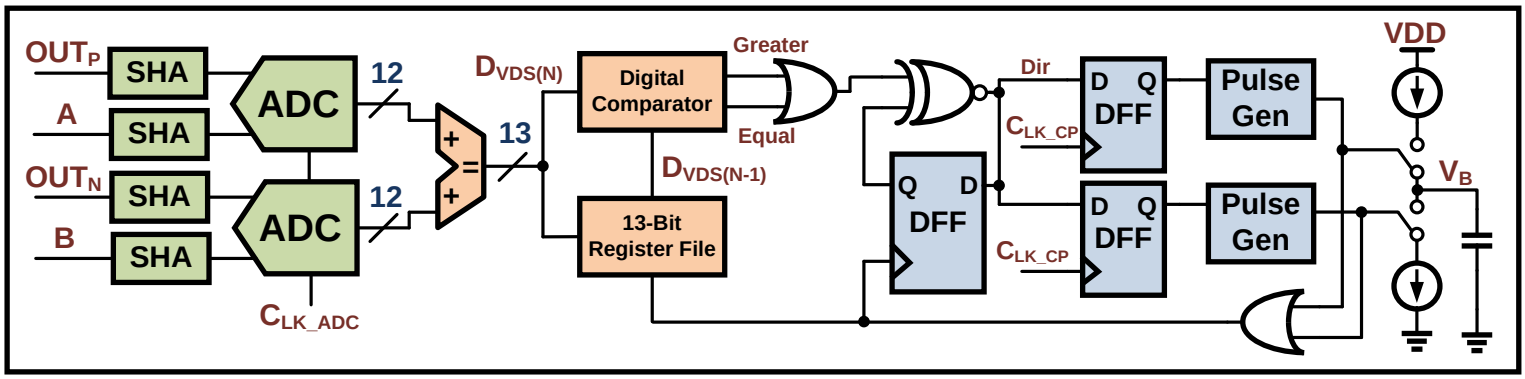

Figure 9: Digital Calibration Block Diagram with A/D Blocks in Green, Digital Word Processing in Orange, and Charge Pump Pulsing in Blue

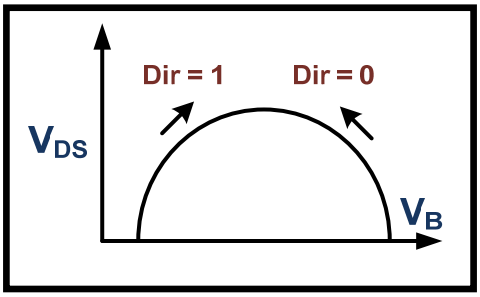

Figure 10: "Dir" Digital Bit Illustration

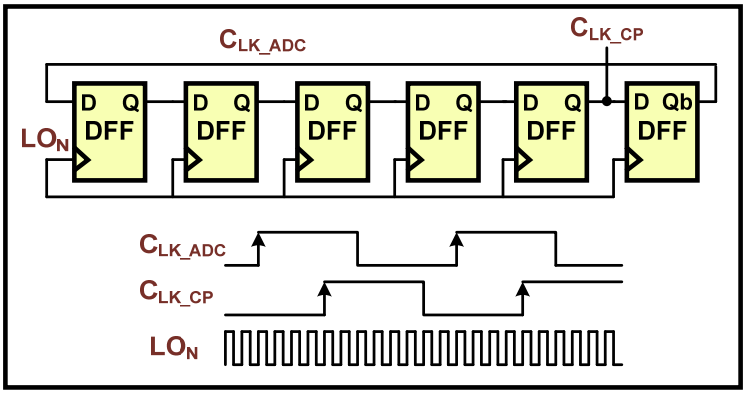

Figure 11: Digital Clocking Scheme

The digital calibration engine implantation is shown in figure 9. The voltage difference from each output and switching nodes are first digitized (green in figure 9). This digitization takes place in order to compare the current voltage with past values and maximize this voltage. A full A/D conversion is implemented rather than a simple comparison with a previous analog value in order to reduce the need for a large DAC.

The input voltage in this case must be sent through a sample and hold buffer before being sent to the ADC due to the large input capacitance of the ADC and the potential kickback from the first stage comparators. The sample and hold amplifier bandwidth will set the maximum frequency the digital block can operate at. The ADC resolution needs to be only 10-12 bits depending on the amount of flicker noise reduction desired. This makes Nyquist rate ADCs a good choice. Pipelined ADCs would work well down to about 50 Mhz after which a SAR ADC would provide lower energy per conversion step.

After being digitized, the two digital input voltages are added (effectively averaging) and compared with the previous digital word (orange section). The digital comparator will output a greater signal (1 = greater, 0 = less) and an equal signal (1 = equal, 0 = not equal). Here the equality and inequality operation were implemented separately, but they could be implemented together by simply subtracting the two digital words and examining the sign bit. After one calibration cycle has been run, the register file is clocked and the old voltage word is erased by the new one.

Following the determination of whether the Vds input is greater or less then the past input, this result is XORed with the previous direction "Dir." The direction is defined in figure 10 as whether the previous Vds was larger than its previous word.

The direction operator ensures that the Vds output will always seek the maxima. For example, if the "Dir" bit is 1 and the current word is greater than the previous, the Vb will increase further which is towards the maxima. This algorithm works well as long as Vds is monotonically increasing until the maxima, and monotonically decreasing after the maxima. This is true for this situation, but when simulated with transient noise, it may not always be the case. However, over time, the noise will average out and the maxima will be reached.

Once the current direction is determined, a pulse is created and sent to the charge pump to either increment or decrement the voltage Vb. In this design, a 30pF capacitor was chosen at the output of the charge pump as a compromise between settling time and noise tolerance (mostly kickback noise).

In the simulated implementation, two charge pumps were added with some additional logic to turn off one charge pump after the Vds value had settled. This allowed for greater resolution in determining the final Vds and lowering the resultant flicker noise.

For high frequency mixers, it's essential that the digital calibration be run slower than the mixer itself, mainly to satisfy timing and power requirements of the ADC and SHA. In this design a simple Johnson Counter was implemented as a frequency divider to clock the digital engine (figure 11). This works well for low division ratios, but for higher division ratios, a more compact divider should be used. The Clk_CP is strobed after CLK_ADC to allow the ADC bits to be resolved and settled.

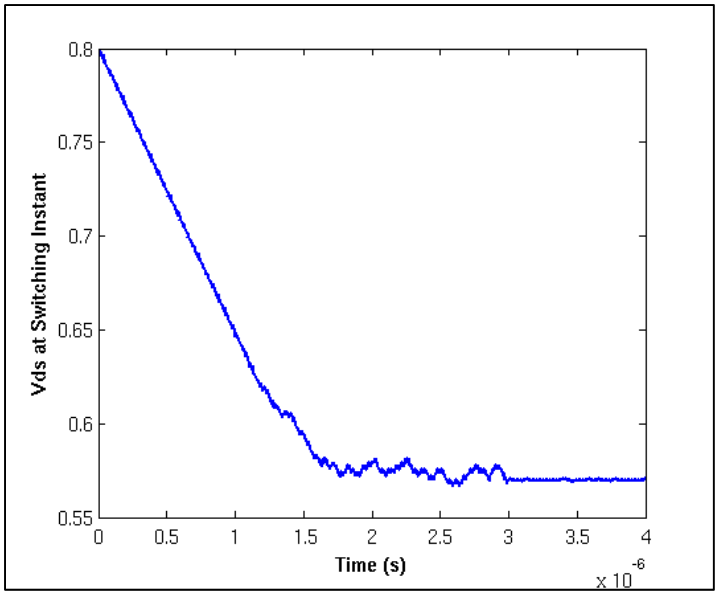

Figure 12: Automatic Calibration Algorithm Convergence

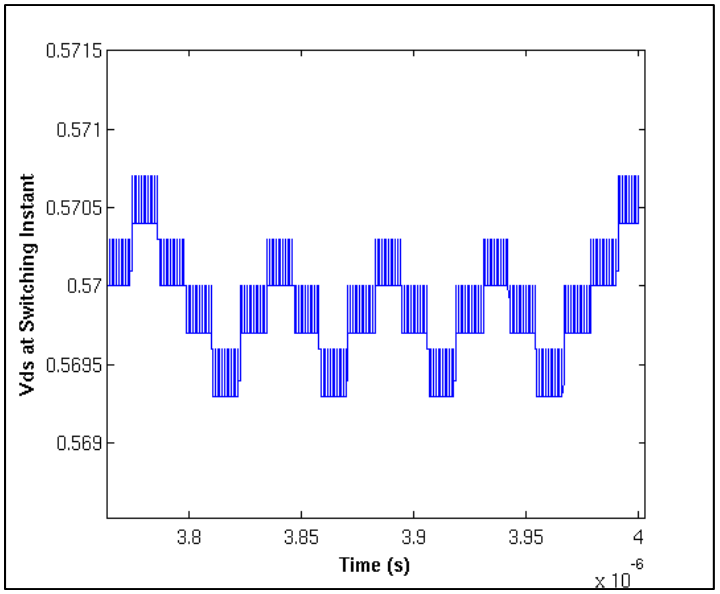

Figure 13: Calibration Algorithm Convergence (Zoomed in at End)

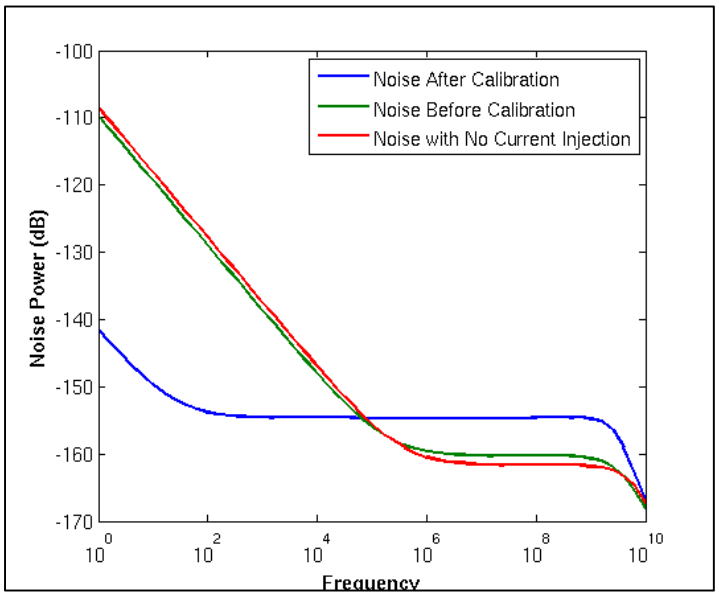

Figure 14: Noise Power Vs. Frequency

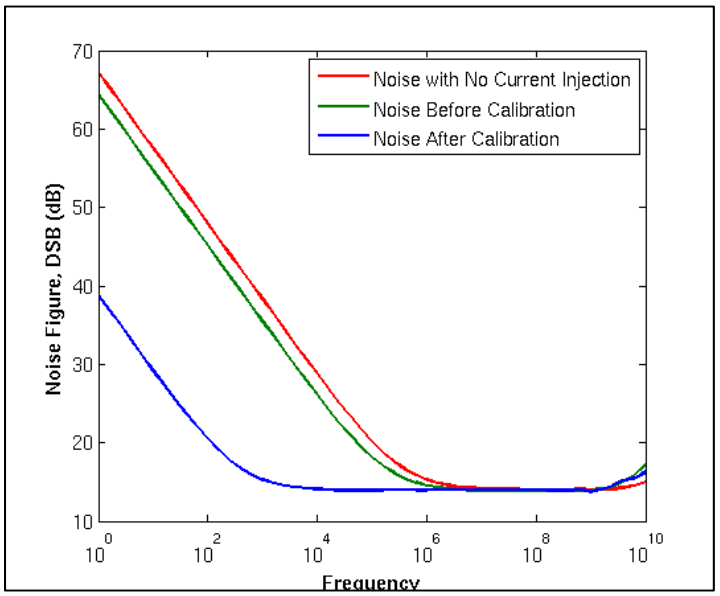

Figure 15: Double Side Band Noise Figure Vs. Frequency

VI. Simulation Results

The proposed implementation was simulated by constructing CMOS mixer as shown in figure 7 with switch and input transconductor sizes at 40u/100n. These sizes were matched to simply the design (sine the focus was on flicker noise reduction). The current injection switches were sized at 40u/200n to increase the threshold of the device to allow for easier turn on. The calibration digital logic was implemented in verilog-A blocks for the proof of concept and simulated using Spectre with transient noise added with a 1Ghz bandwidth. The input LO frequency was a sine wave with a full-scale magnitude at 1Ghz. While this might be a higher than normal frequency for a direct conversion mixer, it was used to test the limits of the calibration scheme. The input RF signal was a 1Ghz +100k Hz simply for simulation speed, however the noise at 100Hz was also examined.

Figure 12 shows the calibration response for an arbitrary starting Vb of 800mV. After three micro seconds, in the calibration logic, one of the charge pumps is removed to allow for finer resolution which gives the flattening seen in the figure. Figure 13 shows a zoomed in version of the settled calibration response. Notice that there is still a great deal of kickback on the bias capacitor and a larger value than 30pF may need to be chosen in practice.

The noise power before and after calibration can be seen in figure 14 while the double side noise figure is shown in figure 15. One thing to note is that while injection lowers the flicker noise corner, it also increases white noise. However, as can be seen in figure 15, this has little impact on the noise figure in that region. The results in figure 15 also tend to align with those of [4] showing the success of the calibration unit.

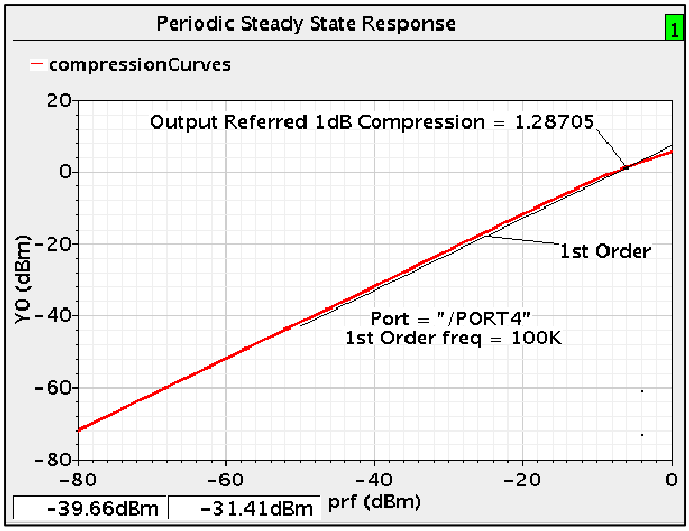

Figure 16: Output Referred 1-dB Compression Point Without Calibration

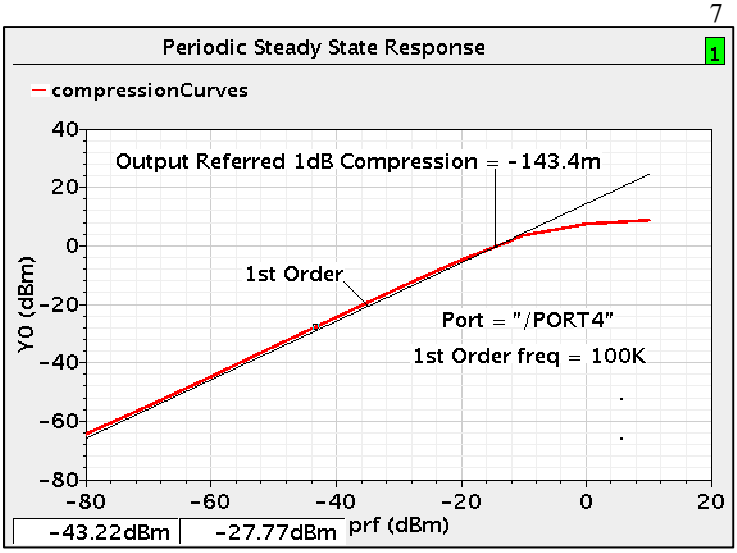

Figure 17: Output Referred 1-dB Compression Point With Calibration

TABLE I
MIXER PERFORMANCE SUMMARY

Parameter	With Calibration	W/O Calibration
Noise Power @ 100Hz (dB)	-154	-128
NF @ 100Hz (dB)	20.5	47.9
Flicker Noise Corner (Hz)	≈ 100	≈1E6
White NF (dB)	13.91	13.89
Conversion Gain (dB)	15.5	8
IIP3 (dBm)	-3.18	3.96
1-dB Compression (dBm)	-.14	1.29
Analog Power Consumption	3.17mW	2.73mW

The 1-dB compression point for the calibrated and un-calibrated mixers is shown in figures 16 and 17. The current injection scheme and increased output swing both add some non-linearity, though this is not significant. The IIP3 is also similar in both cases with the calibrated circuit being slightly worse.

Conversion gain was found to be slightly greater with calibration as shown in table 1. This is most likely due to the increase in output voltage during switching transitions with the current injection. Finally, the analog power consumption of the mixer increased slightly with the injection circuitry. Digital calibration logic will also add some power, however since it is all dynamic (including the ADC) and can be clocked slowly, this should be negligible. Also in reality, the mixer output will already be digitized by a backend ADC to go to the DSP for processing, thus the only additional data conversion power would be in digitizing the switching node.

VII. CONCLUSION

A novel self-biasing calibration technique has been demonstrated for injection based flicker noise reducing down conversion mixers. This scheme determines the optimal flicker noise point by designing the mixer to have a flicker noise minima at the point where the switching transistor Vds is maximized. This maxima can then be determined with a digital background calibration, resulting in a reference free flicker noise reduction implementation. The flicker noise corner was found to reduce by about 4 orders of magnitude and the noise figure at 100Hz dropped by over 20dB.

VIII. REFERENCES

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IX. AUTHOR

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During the Summer of 2008 he was with Teradyne Corp developing high frequency signal tracking and active power management solutions for semiconductor test devices. During the 2007 he was with Intel Corp. investigating high performance, small form factor motherboard architectures to support future PC microprocessor requirements. He is currently a research member of the Analog and Mixed Signal group at Oregon State University in Corvallis, Oregon with a focus in the areas of deep-submicron, low-voltage Analog to Digital Conversion and continuous time filters.

Mr. Guerber is a life member of the Eta Kappa Nu Electrical Engineering Society, an Active Wikipedia Electronics Contributor and is active in his local church.