

A 1.3V Low Power Divide by 4 PLL Design with Output Range 0.5GHz-1.5 GHz

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Abstract— The design and simulation of a divide by four phase locked loop (PLL) operating from 500 MHz to 1.5 GHz is presented. The design has a phase noise of less than 0.2% of the minimum period and a power dissipation less than 318 μ W of power. The PLL is simulated using a TSMC-0.18 μ m CMOS process with a supply of 1.3 V. The PLL was optimized for low power while maintaining reasonable noise characteristics.

I. INTRODUCTION

The demands on the speed and accuracy of integrated circuits has been increasing rapidly in the past few decades. These demands translate into faster clocks with less noise and lower power. Phase locked loops (PLLs) generating and dividing these clocks must therefore be designed with ever tighter specifications.

This report will detail the design of a divide by 4 PLL operating from 500 MHz to 1.5 GHz. The phase noise of this design is less than 0.2% of the operating period and the power is maintained below 320 μ W. The first section of this report will discuss the overall architecture of the PLL and specification for the circuit. The following sections will discuss the design of each PLL sub-block and overall conclusions.

II. DESIGN CHOICES AND OVERALL PERFORMANCE

The design requirements for the given PLL are given in Table 1. To meet these requirements and minimize power, a simple type II structure shown in Figure 1 was chosen. The system was designed by first assuming a loop bandwidth of 12.5 MHz since this was 10 times smaller than the lowest reference frequency (to ensure stability). Assuming a phase margin of 60° (to allow margin for component variations and timely step response settling), we were able to find the ideal loop transfer function and size components such as the loop filter and charge pump. Other components such as the PFD and VCO were chosen to minimize power and phase noise.

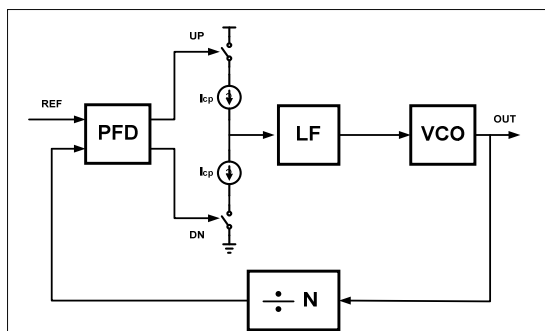


Figure 1: Phase Locked Loop Overall Block Diagram

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TABLE I
PHASE LOCKED LOOP DESIGN REQUIREMENTS

Parameter	Specified Value
Supply Voltage	< 1.8v
Operating Frequency	500MHz to 1.5 GHz
Fixed Feedback Divider	4
Absolute Jitter	0.2% of period (rms)
Power Consumption	Minimum

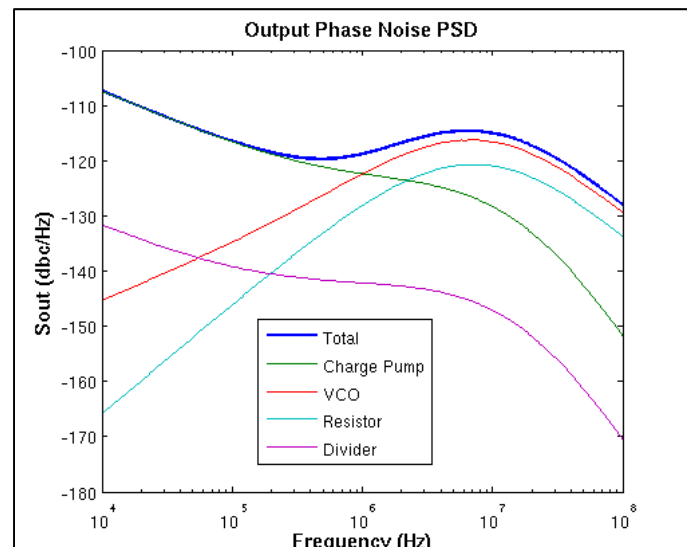


Figure 2: Phase Locked Loop Integrated Phase Noise

The PLL had a phase noise of 0.17% of the high frequency period and the integrated noise is plotted in Figure 2. This noise was minimized due to the architectural choices of the individual blocks (to be described in the following sections) and the initial bandwidth choice. A higher bandwidth could reduce noise from the VCO but would not necessarily help reduce the charge pump noise.

The final power of the PLL was minimized to a final value of 230.46 μ W at 500 MHz and 318.12 μ W at 1.5 GHz. As the PLL was being designed, power was optimized by reducing logic sizes, lowering the supply voltage to 1.3V, reducing VCO power at the expense of phase noise, removing unneeded buffers, minimizing bias ratios, and many hours of transistor level manipulation. The final power was calculated by averaging the current from a long transient response and multiplying that with the supply. A breakdown of where the power went is shown in Figure 3. Note that the charge pump power is much higher due to the choice of I_{cp} (charge pump current) and could be lowered with a redesign of the PLL but was not done here due to time constraints.

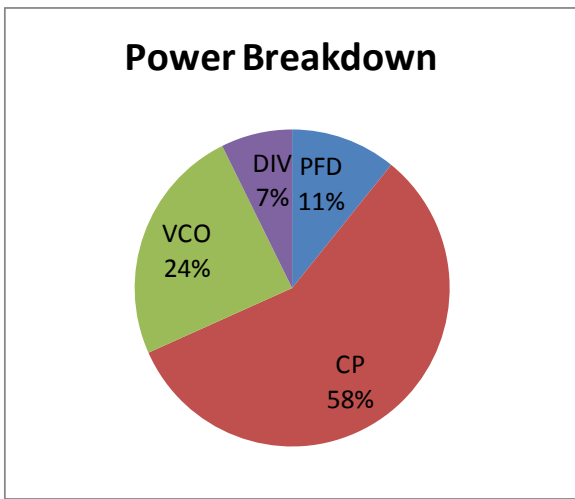


Figure 3: Phase Locked Loop Power Breakdown

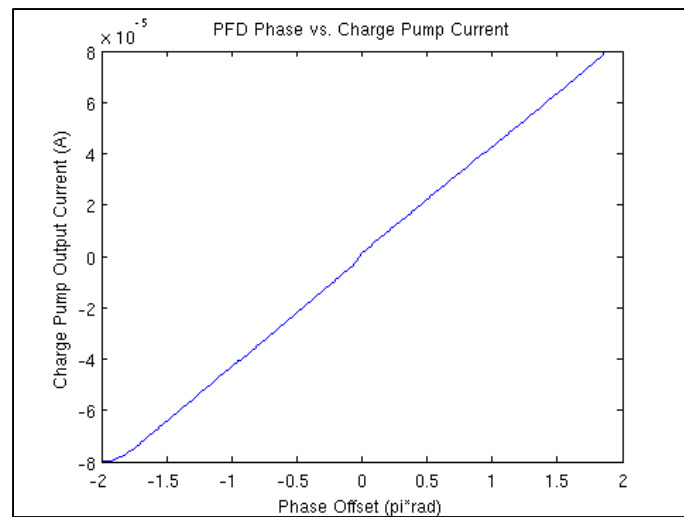


Figure 4: Phase Frequency Detector Gain (KPD)

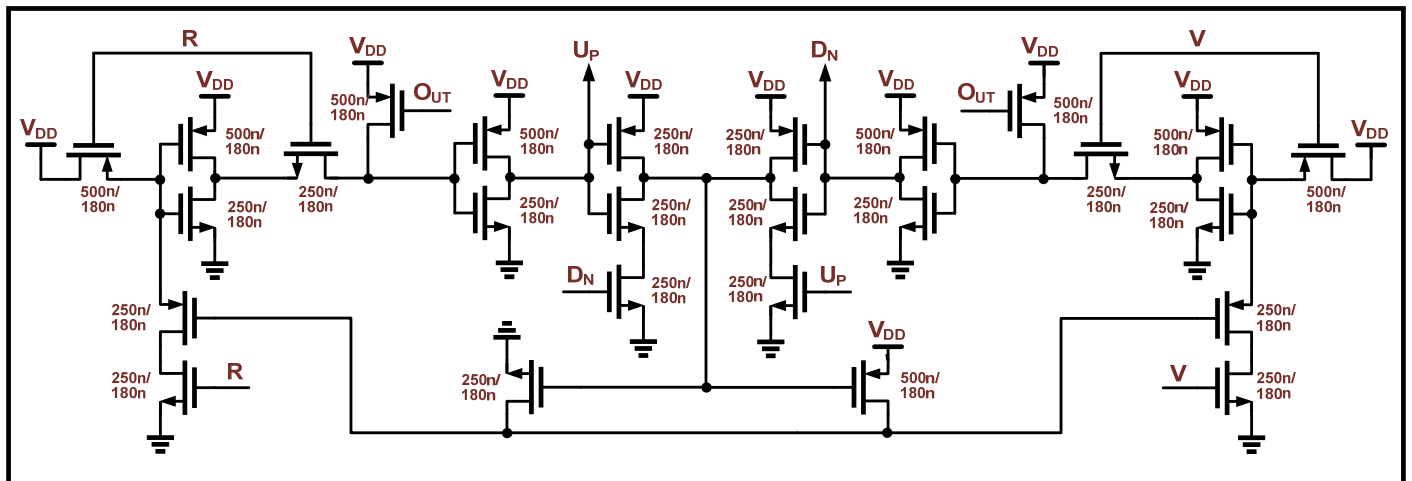


Figure 5: Phase Frequency Detector Transistor Level Schematic

III. PHASE FREQUENCY DETECTOR DESIGN

One of the most important block for controlling the feedback of the PLL is the Phase Frequency Detector (PFD). The PFD was chosen over simple phase detectors due to the ability to differentiate between positive and negative phase differences rather than just the magnitude. This allows for greater range and coarse frequency detection.

The PFD is simple to make and is often represented with two D Flip Flops and a NAND reset gate. There are many architectural variations on this basic design and the variation chosen for this project was the pass-transistor PFD. This PFD is generally the lowest power among common designs although it does not have the range of PFDs such as the glitch latch. However, this range was not needed due to feedback divider.

The simulated gain of the PFD is shown in Figure 4 with the maximum output current equaling the maximum charge pump output of 84uA. It should be noted that this and other phase detectors don't have a full range of 2π , but rather roll off slightly before due to the finite reset time of the PFD and charge pump.

The full PFD schematic is shown in Figure 5. Note that the logic sizes have been minimized greatly to reduce power and area.

IV. LOOP FILTER DESIGN

The loop filter plays the role of minimizing ripple from the charge pump, setting the bandwidth of the PLL, and controlling the stability of the overall PLL loop. The loop filter architecture was chosen to be a passive Proportional Integral (PI) filter for both low power and type II operation. The integral path ensures that cycle slipping can lead productively towards a locked state for the PLL. The loop filter schematic is shown in Figure 6. Component values were chosen to place a zero at the unity gain bandwidth of the PLL loop gain to ensure stability, as seen in Figure 7. Finally, the lone capacitor in the loop filter was sized to place a pole about a decade past the zero to further reduce ripple and deterministic jitter from the resistor.

Sizes for the PI filter were chosen from Equation 1 below by solving for sizes that would ensure proper unity gain bandwidth and phase margin for the loop.

$$F(s) = \frac{s + \frac{1}{RC_1}}{C_2 s \left(s + \frac{1}{R \left(\frac{C_1 C_2}{C_1 + C_2} \right)} \right)}$$

Equation 1 : Loop Filter Transfer Function

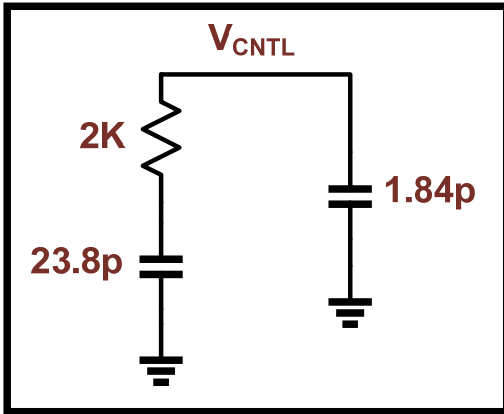


Figure 6: Loop Filter Schematic

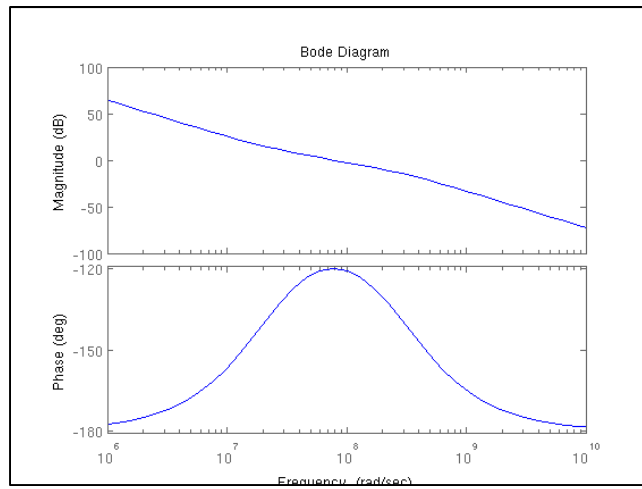


Figure 7: Ideal Loop Gain and Phase

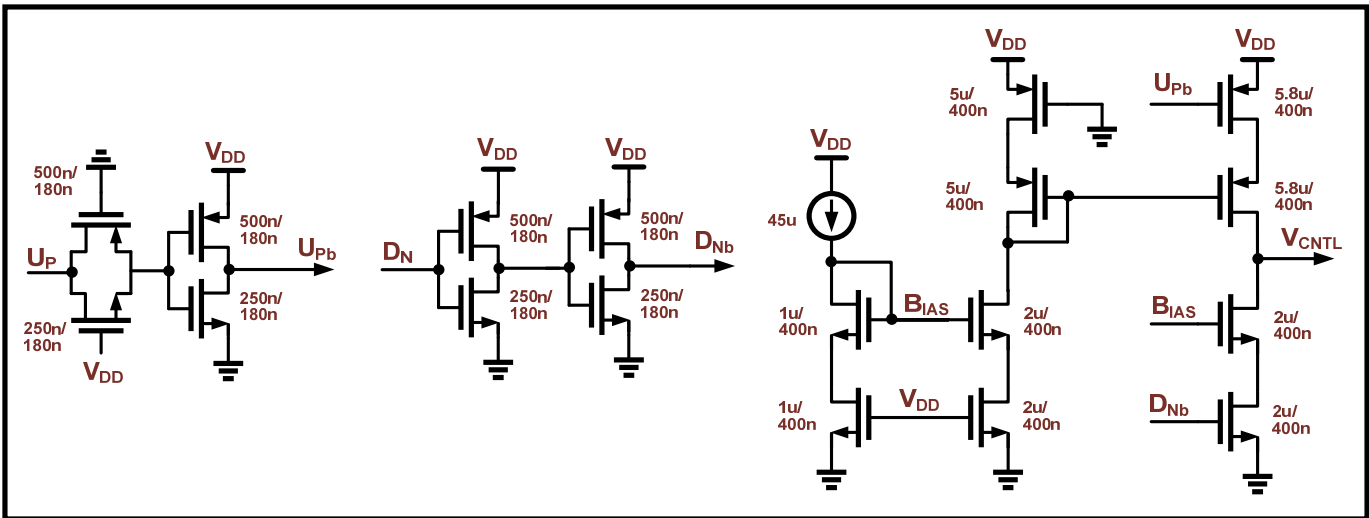


Figure 8: Charge Pump Transistor Level Schematic

V. CHARGE PUMP ARCHITECTURE

The charge pump takes the digital output from the PFD and converts it into a physical control voltage that is delivered to the VCO after being filtered by the loop filter. The architecture chosen for charge pump was a simple switched current mirror as shown in Figure 8. Other architectures were rejected for their power consumption (since deterministic jitter was not a design specification). The output of the charge pump is a $\pm 84\mu\text{A}$ pulse whose period is dictated by the PFD. The fact that the charge pump had to deliver $84\mu\text{A}$ was a limiting factor in the reduction of overall power and could be redesigned with a smaller output current for lower power. The buffering before the UP and DN pulses arrive in the charge pump is to reduce dead zone and reduce the rise and fall times of the controls. This section consumed about $180\mu\text{W}$ of power.

The noise of the charge pump was simulated with a cadence noise analysis on the output current. This was then scaled by the reset time because one can assume that when the PLL is in lock, current will only flow for a period dictated by the reset pulse width. The charge pump ended up not contributing greatly to the noise, only contributing 5% of the total integrated phase noise. The plot of this noise contribution is shown in Figure 2.

VI. VOLTAGE CONTROLLED OSCILLATOR

The Voltage Controlled Oscillator (VCO) creates an oscillation whose frequency is related to the control voltage by the factor K_{vco} . For this PLL, the VCO was designed to minimize power while keeping phase noise to a reasonable limit. The architecture of the VCO is shown in Figure 9 and consists of a simple three inverter ring. This structure was determined to be the lowest power for a given phase noise. To control the ring, a simple PMOS pass transistor was used since a buffered control with opamp would consume too much power. Due to the use of a pass transistor, the range of operation from the control voltage was limited, resulting in a rather high K_{vco} as can be seen in Figure 10. This resulted in slightly higher phase noise and had to be taken into account during the design.

Due to the aggressive power minimization of the VCO block, nearly 72% of the total integrated phase noise came from this block. While high, one can see the result by noting that the VCO only consumed $77\mu\text{W}$ of power operating at 1.5 GHz. In order to reduce low frequency noise, the pass transistor was not chosen to have a slightly larger length than normal while the inverters were all sized small for power.

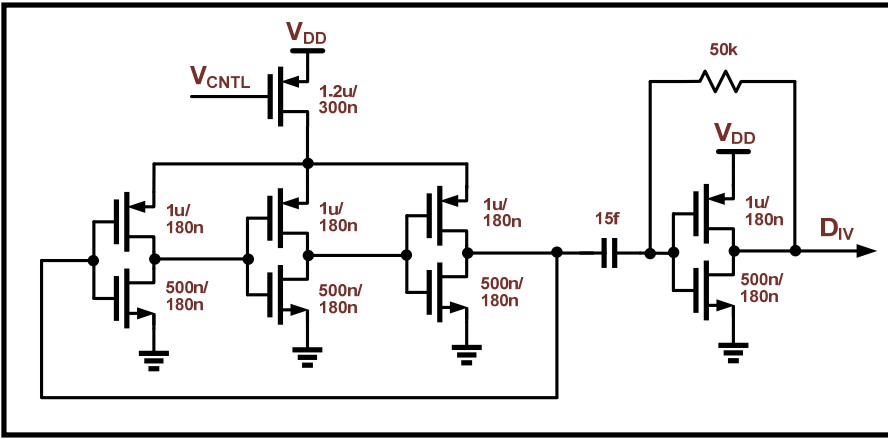


Figure 9: VCO Transistor Level Schematic

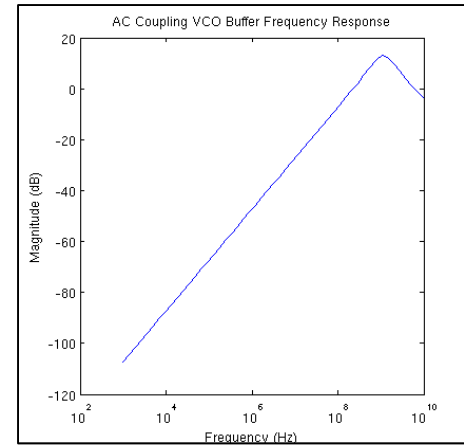


Figure 10: AC Coupling Frequency Response

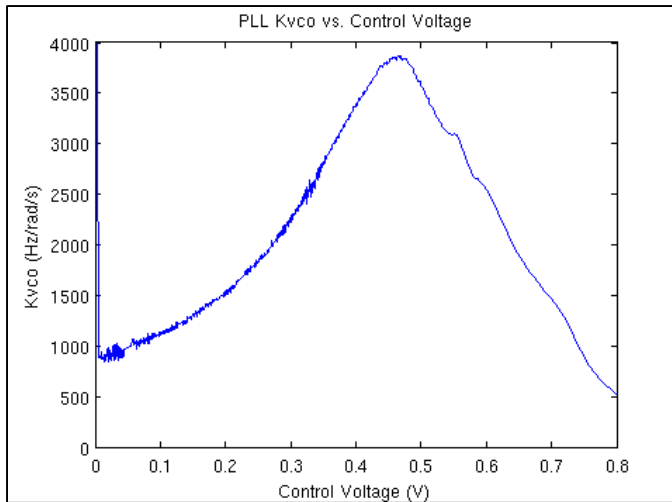


Figure 11: KVCO vs. Control Voltage

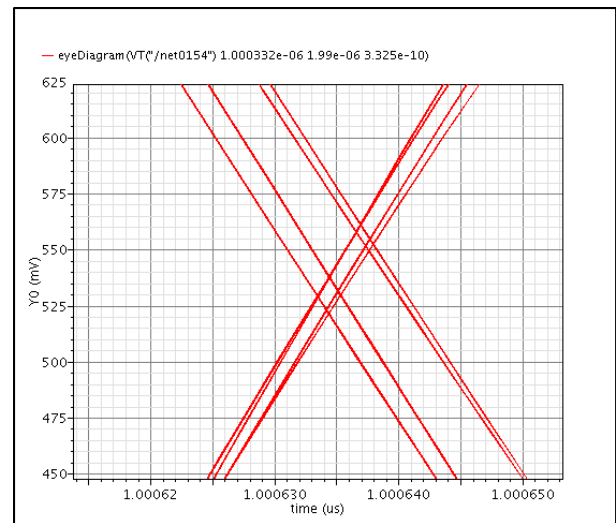


Figure 12: Output Eye Crossing (Deterministic Jitter)

The buffering of the VCO was chosen to only consist of an AC coupling device in order to reduce power. The sizes of the AC coupling circuit were derived by examining the differentiator transform function created by the coupling capacitor and resistor. The goal was to size both of these to allow the high pass transfer function to pass all needed output frequencies while eliminating low frequency offsets. Figure 10 shows the final transfer function of this buffering stage.

The output of the VCO buffer is taken as the output of the PLL. While only limited buffering was performed, the transient response look fairly normal as can be seen in Figure 13. The deterministic jitter, as seen in Figure 12 was larger than expected due to VCO and charge pump minimization, but was kept in check due to the buffering of the VCO and loop filter choice. The final deterministic jitter was measured to be about 3ps peak to peak.

VII. DIVIDER STRUCTURE

The divider circuit performs the operation of reducing the frequency of the VCO output by a factor of four before feeding it back to the input of the PFD. This reduces the speed and power requirements of the PFD while reducing the overall loop gain.

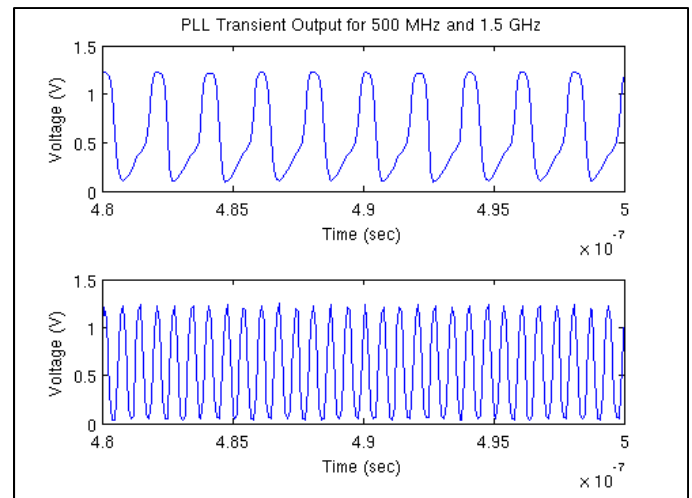


Figure 13: PLL Transient Output Signal

While many divider structures exist, a digital approach was used for this project consisting of two D Flip Flops as shown in Figure 14. The circuit was designed to use as little power as possible while maintaining functionality, thus device sizes were made very small. Also, we discovered that if the divider is configured in the method shown in Figure 14, one inverter branch can be saved, reducing the overall power by nearly 5uW.

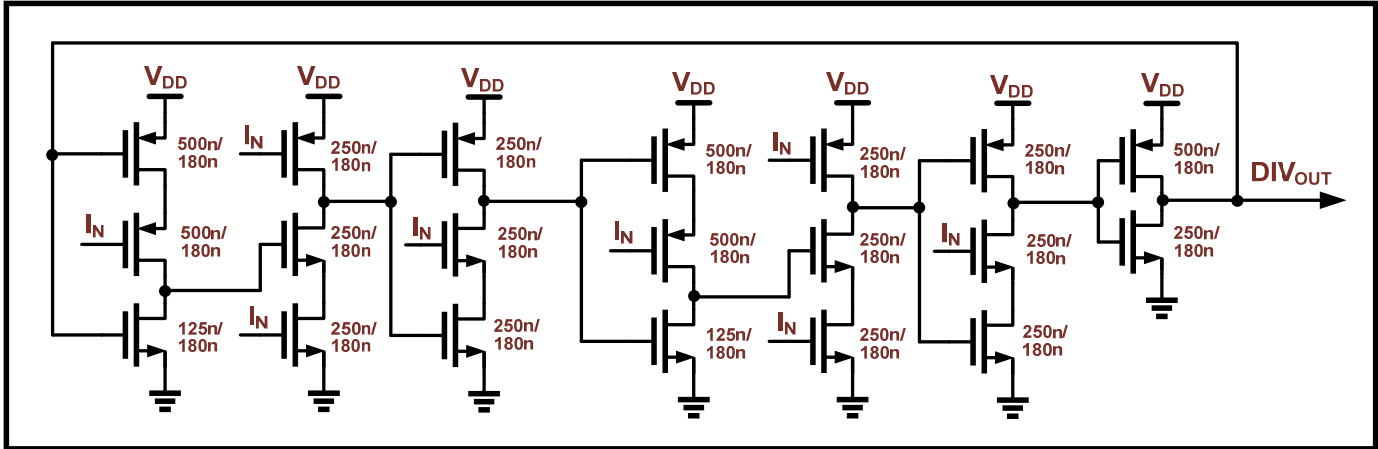


Figure 13: Divider Transistor Level Schematic

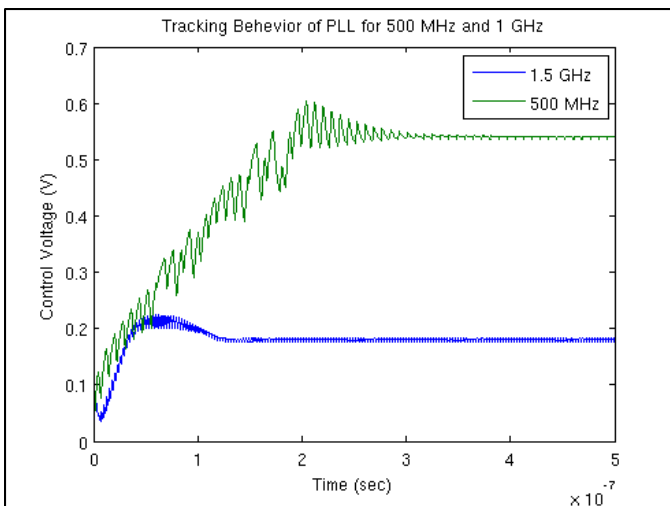


Figure 14: PLL Tracking Response

VIII. PLL CONCLUSIONS

This project has demonstrated the low power design of a divide by four PLL with less than 0.2% phase noise. Novel items in this design include the reduction of divider logic for power savings and the intense power optimization performed on the VCO and PFD structures. A summary of PLL specification can be seen in Table 2 while the locking behavior of the PLL is shown in Figure 13.

From this project it has become clear that power and phase noise will often directly trade and the power limit of a PLL will be dictated by the noise that can be tolerated. Since most of the PLL operation is digital in nature, it was seen that significant power savings can be achieved with the reduction of supply voltage with little functionality implications. A real implementable PLL would need to take into account many more considerations such as supply noise and locking behavior; however this project outlines the fundamental design choices and optimization techniques. These skills can now be applied to designing the next class of mixed signal circuits to push the barriers of electronic design.

TABLE IV
PERFORMANCE SUMMARY

Parameter	Value
Operating Frequency	500 MHz to 1.5 GHz
Supply Voltage	1.3V
KPD	13.36 $\mu\text{A}/\text{Rad}$
Max KVCO	3.8 GHz/Rad/s
Maximum Lock-In Time	300ns
Deterministic Jitter	3ps Pk-Pk
Absolute Jitter (500 MHz)	0.17%
Absolute Jitter (1.5 GHz)	0.16%
VCO Int. Noise. % (of Total)	72%
CP Int. Noise. % (of Total)	5%
RES Int. Noise. % (of Total)	23%
DIV Int. Noise. % (of Total)	0.0361%
Total Power (1.5 GHz)	318.12 μW
PFD Power (1.5 GHz)	34.3 μW
CP Power (1.5 GHz)	183 μW
VCO Power (1.5 GHz)	77.7 μW
DIV Power (1.5 GHz)	23.2 μW

IX. REFERENCES

- [1] P. Hanumolu, "ECE 599 – Phased Locked Loops I," Class Notes, 2009.
- [2] D. Johns and K. Martin, "Analog Integrated Circuit Design," John Wiley Publishing, pg. 119, 1997.