Jon Guerber

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Purpose   Currently a graduate PhD research assistant looking for full-time employment in the mixed signal circuit design field focusing on but not limited to ADCs, interface circuits, clocking, and custom digital design.

Education

Current Educational Status:

Oregon State University, Corvallis, Oregon

PhD (In Progress), Electrical Engineering   Focus area: Analog and Mixed Signal ICs

Current Graduate GPA: 3.97   Expected Graduation Date: November 2012

Major Professor: Dr. Un-Ku Moon

Past Education:

Oregon State University, Corvallis, Oregon

Bachelor of Science, Electrical Engineering, Summa Cum Laude

GPA: 3.93   Graduation date: June 2008

Presidential Scholar, Honor Roll all terms, National Merit Commended Scholar

Clackamas High School, Clackamas Oregon

GPA: 4.0   Graduation date: June 2004   Valedictorian

Design Experience and Coursework

Mixed Signal ICs: Design, simulation, layout, and testing experience using Cadence Virtuoso, Spectre, and Hspice. Designed opamps, comparators, sample and hold structures, ADC structures, basic filters, and digital circuits.

PCBs: Design, schematic, and layout experience using Cadence Allegro, Concept, Advanced Circuits, and Pspice.

Simulation and Validation: Experience with MATLAB, Simulink, Visual Basic, and Excel macros. I have used oscilloscopes, probe stations, logic analyzers, and signal generators.

Digital Programming Experience: Programmed or simulated with Verilog, Modelsim, Assembly Language, understand C Programming, and designed websites in HTML.

Industry Experience: Contributed to PCB board revisions, worked with IC fabrication houses, and proficient in Visio.

Relevant Courses: CMOS Circuit Design, Semiconductor Fundamentals, IC Fabrication, Filters and Network Theory, Analog and Digital Communications, Data Converters, Phase Locked Loops, Radio Frequency Integrated Circuits, Switched Capacitor Design, Digital CMOS Design, Serial Links, Computer Architecture, and Transmission Lines.

Projects

Feedback Initialized Ternary SAR ADC (FITSAR)   2011-Present   (Mentor: Dr. Un-Ku Moon)
- A nested SAR structure is demonstrated that will optimally reduce DAC power and improve accuracy for high efficiency mid-speed and resolution (10-14 bits and 10-100MHz) analog to digital conversion.

Resolution Improvements though PDF Residue Shaping in Redundant Pipeline and SAR ADCs   2010-2011   (U. Moon)
- PDF residue shaping has been demonstrated to improve resolution by utilizing existing 1.5b/stage redundancy structures in multi-stage ADCs even in the presence of sub-ADC offsets.

A 10-bit Ternary SAR ADC (TSAR) with Decision Time Quantization Based Redundancy   2009-2011   (U. Moon)
- A SAR ADC is designed with a novel time based redundancy scheme to reduce power and improve speed.

1-GHz, 9-T, Current Steering SRAM with Decision Feedback Equalization   2009   (Mentor: Dr. Patrick Chiang)
- A 9-T Current Steering approach was used for SRAM reading, with DFE reducing BER for highly capacitive bitlines.

Built In Self Test for Periodic Circuits Using a Beat Frequency Test   2007-2008   (Mentor: Dr. Pavan Hanumolu)
- A beat frequency test unit was designed to detect high frequency periodic signals without the nyquist rate analog to digital conversion and was reconstructed using a simple computer program.

Work experience

Circuit Design Intern, Sensor Products   January 2011 to March 2011
Texas Instruments. Tucson, AZ
- Worked on the IC translation to a higher density process node of a Local/Remote temperature sensor core
- Characterized and optimized a Delta Sigma ADC, Reference generator, and local temperature sensing blocks

Electrical Engineering Intern, Semiconductor Test Development   June 2008 to September 2008
Teradyne Corp.   Tualatin, Or
- Developed and validated a board level voltage and temperature monitoring system
- Assisted in implementing signal tracker functionality for improved accuracy and functionality of high speed data circuits
- Validated signal integrity and power distribution on main channel PCB boards
- Contributed to schematic and layout updates for board revisions

Electrical Engineering Intern, Platforms and Systems Technology   April 2007 to September 2007
Intel Corp.   Hillsboro, Or
- Ran SPICE circuit simulations of test structures and assisted with PCB qualifications
- Programmed FPGA using Verilog to replace discrete onboard circuitry
- Worked on PCB layout and motherboard design studies for boards supporting the launch of Intel chipsets

Teaching Assistant, Electrical Fundamentals and CMOS Circuit Design, Fall 2006, Winter 2007, Fall 2007, Winter 2008, Fall 2008, Winter 2009, Spring 2009
Oregon State University   Corvallis, Oregon
- Helped run lab sessions and assisted with teaching and grading for electronics classes

Electrical Engineering Intern, June 2005 to September 2005
InFocus Corp.   Wilsonville, Oregon
- Worked with the reliability engineering department on test projects for projector power supply boards

Facilities Maintenance, Summer 2004, Winter 2004, 2005, 2006
Oregon Cutting Systems   Portland, Or
- Factory maintenance, repair work and product packaging

Selected Publications

- **J. Guerber**, M. Gande, H. Venkatram, A. Waters, U. Moon, "A 10b Ternary SAR ADC with Quantization Time Information Utilization," *IEEE J. Solid State Circuits.* Invited, to appear in Nov. 2012.
- **J. Guerber**, M. Gande, U. Moon, "The Analysis and Application of Redundant Multi-Stage ADC Resolution Improvements Through PDF Residue Shaping," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.,* Accepted.
- **J. Guerber**, M. Gande, H. Venkatram, A. Waters, U. Moon, "A 10b Ternary SAR ADC with Decision Time Quantization Based Redundancy," *IEEE Asian Solid-State Circuits Conf.* Nov. 2011, pp. 63-65.
- **J. Guerber**, H. Venkatram, T. Oh, U. Moon, "Enhanced SAR ADC Energy Efficiency from the Early Reset Merged Capacitor Switching Algorithm," *IEEE Int. Symp. Circuits Syst.*, Accepted, May 2012.
- H. Venkatram, **J. Guerber**, S. Lee, and U. Moon, "Merged capacitor switching based SAR ADC with highest switching energy-efficiency," *Electron. Lett.*, vol. 46, no. 9, pp. 620-621, Apr. 29, 2010.

Professional Affiliations and Awards

IEEE student member (2005-present)
Eta Kappa Nu electrical engineering honor society Vice President, Oregon State University chapter (2007-2008)
Analog devices outstanding student designer award (2012)
Semiconductor research corporation (SRC) graduate fellow (2011-present)

Volunteer experience

Ran the electronic timing system for the pinewood derby model car race for cub scout troop 0258 (2009-2012)
Volunteer home builder in underdeveloped regions of Tijuana and Tecate, Mexico, (Spring 2007 and 2008)
Hurricane Katrina relief worker, Biloxi, Mississippi, (Spring 2006)
Missionary to rural southern Serbia, (Summer 2006) and active in local church
Active Wikipedia contributor (Edited many integrated circuit design pages), promoter of local wikis (2005-present)
Volunteer coordinator for Oregon State EECS graduation ceremony (2007-2012)