Jon Guerber

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Purpose

Currently a mixed signal circuit designer focusing on but not limited to ADCs (SAR, Pipeline, Flash, Delta Sigma), DACs, interface circuits, serial link transceivers, regulators, amplifiers, calibration circuits, and general mixed signal design.

Education

Education History:

Oregon State University, Corvallis, Oregon
PhD, Electrical Engineering — Focus area: Analog and Mixed Signal IC Design
Graduate GPA: 3.97 — Graduation Date: December 2012
Major Professor: Dr. Un-Ku Moon

Oregon State University, Corvallis, Oregon
Bachelor of Science, Electrical Engineering
GPA: 3.93, Summa Cum Laude — Graduation date: June 2008
Presidential Scholar, Honor Roll all terms, American Electronics Association Scholar

Clackamas High School, Clackamas, Oregon
GPA: 4.0 Graduation date: June 2004 Valedictorian, National Merit Commended Scholar

Design Experience and Coursework

Mixed Signal ICs: Design, simulation, layout, and testing experience using Cadence tools, Spectre, and Hspice. Designed ADC and DAC structures, comparators, amplifiers, switches, serial links, calibration architecture and mixed signal circuits.

PCBs and Digital Design: Design, schematic, and layout experience using Cadence Allegro, Concept, Advanced Circuits, and Spice tools. Am also familiar with Verilog, C Programming, HTML, and wiki markup.

Simulation and Validation: Experience with MATLAB, Simulink, Cadence behavioral models, and Excel macros. I have used oscilloscopes, probe stations, logic analyzers, signal generators and designed circuit validation boards.

Industry Experience: Contributed to PCB board revisions, worked with IC fabrication houses, and proficient in Visio.

Relevant Courses: CMOS Circuit Design, Semiconductor Fundamentals, IC Fabrication, Filters and Network Theory, Analog and Digital Communications, Data Converters, Phase Locked Loops, Radio Frequency Integrated Circuits, Switched Capacitor Design, Digital CMOS Design, Serial Links, Computer Architecture, and Transmission Lines.

Selected Publications

- H. Venkatram, **J. Guerber**, M. Gande, and U. Moon, "Detection and correction methods for single event effects in analog to digital converters," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 60, no. 12, pp. 3163-3172, Dec. 2013.
- M. Gande, **J. Guerber**, and U. Moon, "Analysis of Back-End Flash in a 1.5b/Stage Pipelined ADC," *Proc. of IEEE Int. Sym. On Circuits and Systems*, May 2013.
- **J. Guerber**, H. Venkatram, M. Gande, and U. Moon, "Ternary R2R DAC design for improved energy efficiency" *Electron. Lett.*, vol. 49, Feb. 28, 2013.
- **J. Guerber**, M. Gande, H. Venkatram, A. Waters, U. Moon, "A 10b Ternary SAR ADC with Quantization Time Information Utilization," *IEEE J. Solid State Circuits.* Vol. 47, no. 11, Nov. 2012. (Presented at ASSCC 2011)
- **J. Guerber**, M. Gande, U. Moon, "The Analysis and Application of Redundant Multi-Stage ADC Resolution Improvements Through PDF Residue Shaping," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.,* Aug. 2012
- **J. Guerber**, H. Venkatram, T. Oh, U. Moon, "Enhanced SAR ADC Energy Efficiency from the Early Reset Merged Capacitor Switching Algorithm," *IEEE Int. Symp. Circuits Syst.*, May 2012.
- T. Oh, H. Venkatram, **J. Guerber**, and U. Moon, "Correlated Jitter Sampling for jitter cancellation in pipelined TDCs," *IEEE Int. Symp. Circuits Syst.*, May 2012.
- H. Venkatram, **J. Guerber**, S. Lee, and U. Moon, "Merged capacitor switching based SAR ADC with highest switching energy-efficiency," *Electron. Lett.*, vol. 46, no. 9, pp. 620-621, Apr. 29, 2010.
- **J. Guerber**, "Time and Statistical Information Utilization in High Efficiency Sub-Micron CMOS Successive Approximation Analog to Digital Converters" PhD Dissertation, Oregon State University, Department of Electrical Engineering and Computer Science Dec. 2012.

Graduate Research

High Efficiency Nested SAR ADC (previously FITSAR) 2011-2013 (Mentor: Dr. Un-Ku Moon)

- A nested SAR structure is demonstrated that will optimally reduce SAR DAC and comparator power while improving accuracy and speed, based on the concepts of interstage data recoding and feedback initialization.

Resolution Improvements though PDF Residue Shaping in Redundant Pipeline and SAR ADCs 2010-2011 (U. Moon)

- PDF residue shaping has been demonstrated to improve resolution by utilizing existing 1.5b/stage redundancy structures in multi-stage ADCs even in the presence of sub-ADC offsets.

A 10-bit Ternary SAR ADC (TSAR) with Decision Time Quantization Based Redundancy 2009-2011 (U. Moon)

- A SAR ADC is designed with a novel time based redundancy scheme to reduce power and improve speed. This introduces for the first time, full SAR 1.5b/stage redundancy with no added stages and a binary DAC.

Three level R2R DAC Design 2012-2013 (U. Moon)

- DAC power and linearity can be dramatically improved with the use of three level switching and ternary encoding.

Work experience

Analog Integrated Circuit Design Engineer, January 2013 - Present
Intel Corp. Hillsboro, Or

- Analog IC circuit designer of IO, data converters, power management, as well as analog SOC pathfinding

Circuit Design Intern, Sensor Products January 2011 to March 2011
Texas Instruments. Tucson, AZ

- Worked on the IC translation to a higher density process node of a local/remote temperature sensor core
- Characterized and optimized a Delta Sigma ADC, reference generator, and local temperature sensing blocks

Electrical Engineering Intern, Semiconductor Test Development June 2008 to September 2008
Teradyne Corp. Tualatin, Or

- Developed and validated a board level voltage and temperature monitoring system
- Assisted in implementing signal tracker functionality for improved accuracy of high speed data circuits, validated signal integrity and power distribution on main channel PCB boards, and contributed to board revisions

Electrical Engineering Intern, Platforms and Systems Technology April 2007 to September 2007
Intel Corp. Hillsboro, Or

- Ran SPICE circuit simulations of test structures, assisted with PCB qualifications
- Programmed FPGA using Verilog to replace discrete onboard circuitry
- Contributed to PCB layout and motherboard design studies for boards supporting the launch of Intel chipsets

Teaching Assistant, Electrical Fundamentals and CMOS Circuit Design, Fall 2006 to Spring 2012
Oregon State University Corvallis, Or

- Helped run lab sessions and assisted with teaching and grading for electronics classes

Facilities Maintenance, Summer 2004, Winter 2004, 2005, 2006
Oregon Cutting Systems Portland, Or

- Factory maintenance, repair work and product packaging. Learned how to work hard.

Professional Affiliations and Awards

IEEE student member (2005-2013), member (2013-Present)
Eta Kappa Nu electrical engineering honor society Vice President, Oregon State University chapter (2007-2008)
IEEE solid-state circuits society member (2011-Present)
Analog devices outstanding student designer award (2012)
TECHCON best in session award, circuit design (2012)

Volunteer experience

Ran the electronic timing system for the pinewood derby model car race for cub scout troop 0258 (2009-2012)
Volunteer home builder in underdeveloped regions of Tijuana and Tecate, Mexico, (Spring 2007 and 2008)
Hurricane Katrina relief worker, Biloxi, Mississippi, (Spring 2006)
Missionary to rural southern Serbia, (Summer 2006) and active in local church
Active Wikipedia contributor (Edited many integrated circuit design pages), promoter of local wikis (2005-present)
Volunteer coordinator for Oregon State EECS graduation ceremony (2007-2012)