A 10b Ternary SAR ADC with Decision Time Quantization Based Redundancy

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***Abstract*— The design of a Ternary Successive Approximation ADC (TSAR) with decision time quantization is proposed. The TSAR examines the transient information of the typical SAR comparator to provide full half-bit redundancy, an increased monotonicity switching algorithm, speed enhancements without inherent metastability, residue shaping effects, and stage skipping. A prototype is fabricated in 0.13µm CMOS employing on-chip statistical time reference calibration and supply variability from 0.8 to 1.2V. The chip consumes 84µW at 8 MHz for a FOM of 16fJ/C-S.**

I. Introduction

Successive approximation (SAR) ADCs have long been an essential member of the Nyquist ADC family. They specialize in the low power digitization of medium resolution and speed signals for applications such as medical instrumentation, and digital imaging while requiring little area and scaling well with process minimization. Today, SARs are increasingly popular and are being asked to operate at higher speeds with smaller power budgets.

To meet these demands, a number of novel SAR architectures have been proposed that attempt to creatively enhance performance metrics. The asynchronous ADC proposed in [1] increases the effective speed of a SAR conversion by a factor of two. However, the issue of mid-cycle metastability leads to either a larger bit error rate (BER) or increased critical path logic [2]. The variable window function SAR [3] reduces the amount of required switching to achieve the necessary SAR input voltage minimization, but needs additional voltage comparators and fast clocked DACs. Redundancy in the SAR architecture through sub-radix arrays [4] and additional stages [5]-[6] can reduce the settling time requirement of the capacitor bank, and allow for input calibration signals, at the expense of extra cycles and power consumption due to additional comparisons and digital complexity. Finally, merged capacitor switching (MCS) SAR architectures have been demonstrated to maximally reduce switching energy [7]-[8].

In this paper, a new Ternary SAR (TSAR) architecture is proposed that utilizes the MCS SAR transient information to provide enhanced speed, redundancy and reduced power consumption with little overhead. This paper is organized as follows: Section 2 will motivate and describe the TSAR structure, Section 3 will explore the inherent benefits of the architecture, Section 4 will describe enhancements made to the basic TSAR structure, Section 5 includes measurement results, and conclusions will be given in Section 6.

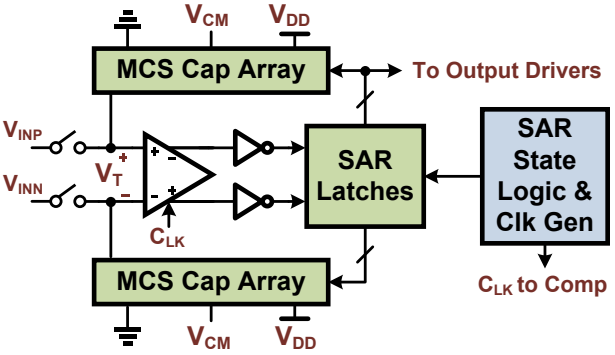

Fig. 1. MCS binary SAR core block diagram [7].

II. Proposed TSAR Architecture

The reduced switching energy MCS SAR is shown in Fig. 1. Assuming that the comparator has a typical single pole response, its respective transient response can be modeled as the following:

$$V_{OUT} = (V_G)exp[(A-1)t/\tau] \quad (1)$$

Where A is the comparator gain, V_G is the comparator input voltage, and τ is the time constant. While exponential in nature, this delay is shown to vary linearly with the full-scale voltage of each stage (which scales down by a factor of two for each stage) in the SAR operation:

$$t_{Stage(N)} - t_{Stage(N-1)} = \frac{ln(2)}{[(A-1)/\tau]} = \frac{ln(2)}{C} \quad (2)$$

This variation is plotted in Fig. 2 from a transient simulation of a dynamic transistor level comparator. Since the delay response is independent of the polarity of the input, measuring the time delay of the comparator gives information about the absolute value of the input.

The proposed TSAR structure is shown in Fig. 3. Here a time comparator and delay unit are introduced into the path of the SAR loop in a differential fashion. The time comparator structure consists of typical back to back inverter latches with reset capability. A delay unit, consisting of a current starved inverter based ring

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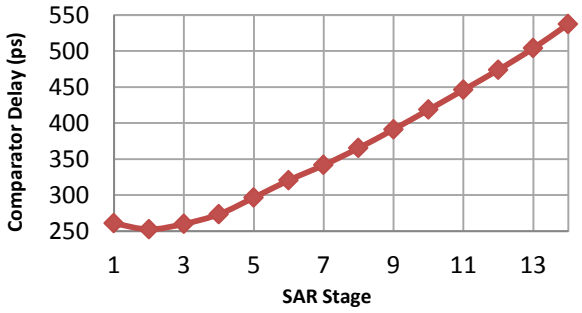

Fig. 2. Comparator delay given an input voltage equal to the full-scale voltage of a SAR stage.

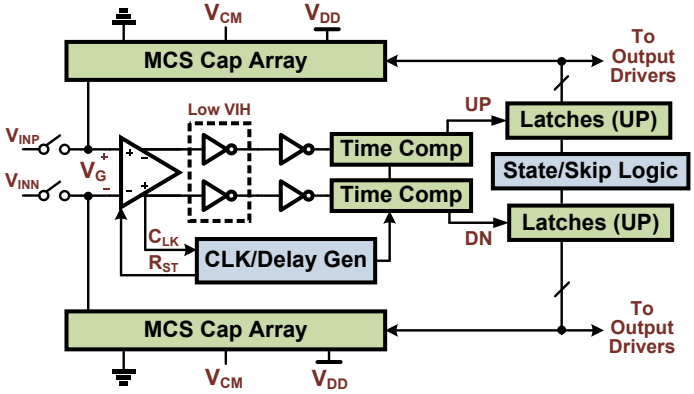

Fig. 3. Proposed TSAR analog core showing voltage comparison, time comparison, data latching, and feedback paths.

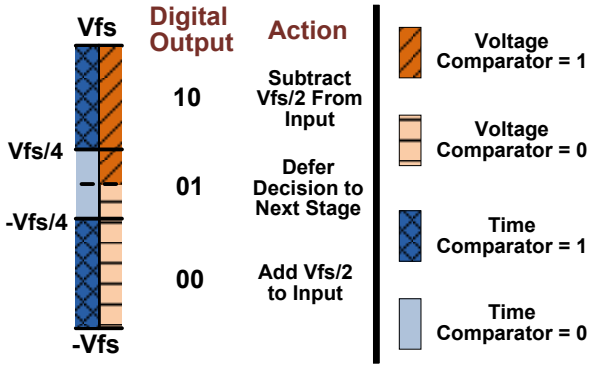

Fig. 4. TSAR stage coding due to voltage and time comparator outputs.

oscillator, provides both the delay to latch the time comparators and internal clocking capabilities for the TSAR loop. Improved SAR state and skipping logic is also present.

The operation of the TSAR core for a sample begins with the master clock sampling the input and delivering a clock edge to the voltage comparator and delay unit. A delayed clock edge is then sent to the time comparator. If the buffered output of the voltage comparator resolves to a high or low value before the delayed clock latches the time comparators, the stage output to the logic and capacitor DAC is the standard '10' or '00' code. However, if the input does not trip the buffer inverters to either a high or low value before the delayed clock, the output will be in the middle region and will be given a '01' digital code as illustrated in Fig. 4.

III. Inherent TSAR Performance Benefits

This ternary coding structure based on time quantization has many inherent benefits, with the first being the presence of an effective 1.5 bit/stage redundancy. This redundancy requires no additional stages or comparators. Furthermore, as with 1.5 bit/stage redundancy in pipeline ADCs, the effective redundant reference levels (here time delays) can vary from Vfs/2 to 0 without having over-range errors in following stages. This voltage domain requirement becomes more relaxed in the time domain since there is a set time value that symmetrically translates to the +/- Vfs/2 level, but not the zero level (i.e. the single comparator voltage offset does not affect redundancy). For the TSAR redundancy level to go to zero, the time delay must be infinite, which is not possible. Since the voltage comparator delay varies linearly with the TSAR stage scaling, there is also no increased time comparator accuracy requirements in later stages as is the case if the redundancy were implemented in the voltage domain. This redundancy has been used to reduce the required settling time after input sampling and DAC switching.

The TSAR time comparator latching also has built in speed benefits. Like the asynchronous SAR, the TSAR does not wait for the worst case delay of the voltage comparator to move on with the rest of the SAR cycle. Rather, after the delayed clock strobes the time comparators, the TSAR loop clocks the critical path logic and DAC, if needed, whether or not the voltage comparator has resolved. This timing structure has benefits over the traditional asynchronous structure in that every cycle is deterministically ended with the delayed clock edge even if the voltage comparator is metastable. While the traditional asynchronous SAR loop will sometimes resolve quickly and other times slowly when the virtual node input is small, the TSAR loop never needs to wait for small inputs, but only for inputs larger than the given stage time redundancy level. Additionally, no fast clock is required as the internal clocking and delay units are combined.

Finally, the TSAR structure also provides an enhanced DAC switching operation allowing the sampled input voltage to monotonically be reduced to zero differentially. Because this reduces the number of switching events to get the same output, the TSAR provides power savings similar to that of [3]. In this case however, the two additional voltage comparators can be replaced by cheap time quantizers. Also, the variable window function can be extended to the whole SAR which, while having minimal effect of capacitor switching energy, will have a noticeable decrease in logic and capacitor buffer power.

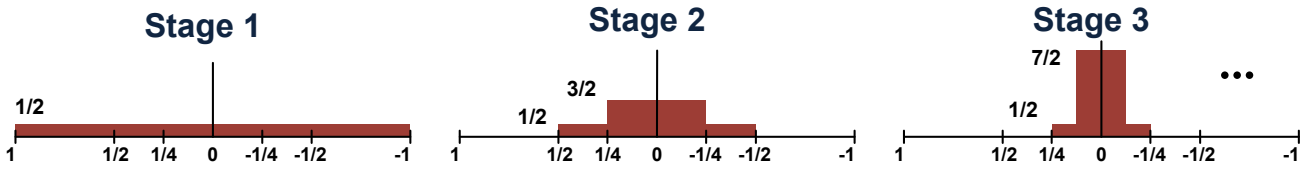

Fig. 5. TSAR Residue Shaping for a Uniform Input PDF

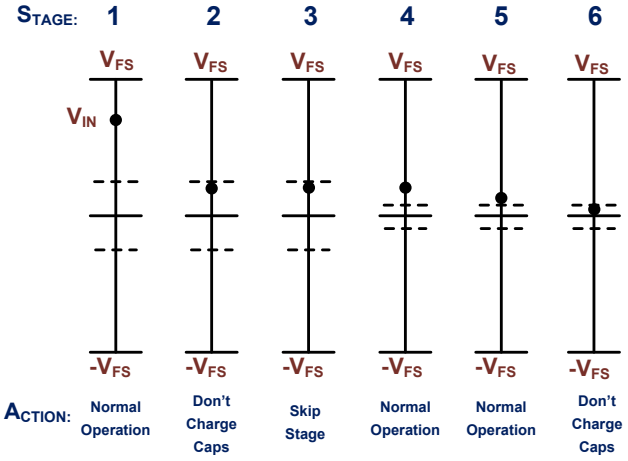

Fig. 6. Stage skipping due to grouped reference levels

IV. TSAR Structural Enhancements

While the TSAR structure has many inherent benefits, the architecture can be further modified to improve performance. First, the observation should be made that unlike binary and sub-radix SARs, the TSAR has a residue shaping feature. This means that given a uniform input PDF, the PDF width of the residue of every stage decreases by nearly 2x (PDF magnitude increases) more than in a binary SAR within the redundancy limits, and the outer most PDF regions remain the same as seen in Fig. 5. For each TSAR stage with redundancy, the probability that the following stage is redundant thus increases. Since the redundancy can shape across the whole range of the SAR, it can be shown that the last stage residue can be squeezed into half the range of a normal binary SAR last stage, resulting in effectively an extra 6dB of resolution.

Not only can residue shaping reduce the number of times the DAC must switch (on average) for a TSAR conversion, but the redundancy levels in the TSAR can be grouped in such a way to reduce the total number of SAR cycles required for an average conversion. This reduction, stage skipping, is illustrated in Fig. 6. If a TSAR stage output is determined to be redundant and the next stage has the same redundancy level (setting the amount of redundancy is flexible in SAR 1.5 bit stages), not only can the current stage DAC switching be skipped, but also all of the following stages until a new redundancy level is introduced.

Stage skipping has many power savings implications because when a stage is skipped, the power from the

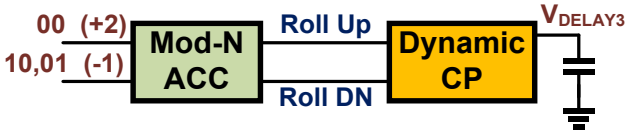

Fig. 7. Background calibration circuit implemented with a digital accumulator and dynamic charge pump for calibrating time reference 3. For a ¼ reference level, 50% of the code should equal "00"

voltage comparator, time comparators, DAC elements, DAC buffers, data latching and even state generator is zero (barring minimal leakage). In order to save the maximum power, through both normal variable window type switching reductions and stage skipping, all possible combinations of time reference groupings with transistor level blocks were simulated and the optimal stage grouping were determined. Due to the TSAR time quantization, residue shaping, and stage skipping, a 10 bit TSAR operation on a uniform input requires, on average, 8.03 operating cycles and 6.53 DAC switching events, with only 3 distinct time reference values. Note that this is in stark contrast to other redundancy schemes which often require up to 1.5x more stages and can have side effects such as non-binary arrays, digital complexity, and extra analog domain signal shifting [4]-[6].

In this TSAR architecture, there are only three reference levels needed to provide all of the circuit redundancy. The first two can be coarse, as their variability has no direct impact on the achievable resolution of the ADC, as long as the time delay is not so short that the voltage domain redundancy level exceeds Vfs/2. The last reference level however controls the final residue shaping and while its variability will only degrade the resolution by at most 6dB, it is preferable to have this level be bounded to within about 3Vfs/8 to 3Vfs/16 in the voltage domain (effective) to maintain 10b resolution with less than 1dB of SQNR degradation. These are still broad reference bounds, and when translated to the time domain, the reference can also be easily set by the statistical background calibration loop shown in Fig. 7. Since the ideal final stage reference level sets 50% of the last stage digital outputs to be redundant (due to residue shaping), the calibration unit accumulates the number of redundant events with a weight of 2 and non-redundant events with a weight of -1. When an accumulation rollover occurs, a dynamic charge pump can increment the reference value held on a capacitor feeding the current starved timing VCO, setting the time reference to provide well under 1dB

of degradation. This calibration operates in the background and counts at 1/64 the master clock rate with rollovers occurring no faster than 1/4096 the clock rate making this power consumption negligible.

V. Measurement Results

The TSAR chip was fabricated in 0.13µm CMOS, taking an area of 0.056 mm² (excluding digital calibration). Performance was measured up to 40 MHz and runs with both 0.8V and 1.2V supplies and plotted in Fig. 8. At 8 MHz and supply of 0.8V the power was 83.8µW, which, with an ENOB of 9.28 resulted in a FOM of 16.8fJ/C-S. Power of the entire SAR is reduced by 26% with time quantization enabled at 8 MHz. Redundancy and calibration match with simulation, and foreground calibration was used for small capacitor errors (for 2dB improvement). Results are summarized in Table 1 and the annotated die micrograph is shown in Fig. 9.

VI. Conclusions

This paper has demonstrated a Ternary SAR ADC with decision time quantization. The TSAR structure increases speed without inherent metastability, improves the monotonicity of the switching algorithm without extra voltage comparators, provides full half bit redundancy with reduced effective stages, and allows for residue shaping and stage skipping.

VII. Acknowledgements

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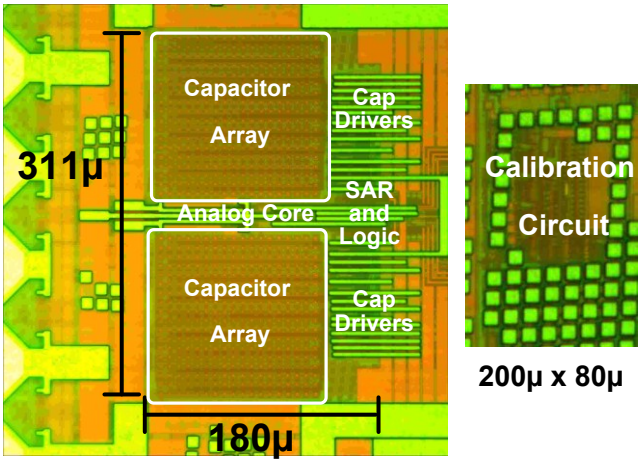

Fig. 9. Die photo of the TSAR core and calibration with a SAR area of 0.056mm² and digital calibration area of 0.016mm².

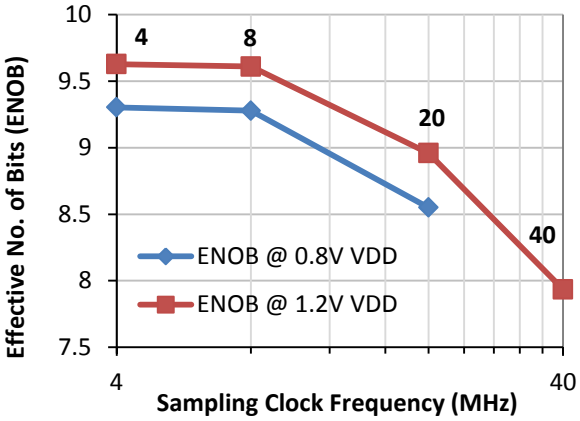

Fig. 8. Measured ENOB vs. sampling frequency for nyquist inputs (fsignal is fsample/2)

TABLE I
TSAR Performance Summary

Clock Freq (MHz)	8	8	20	20	40
Supply (V)	0.8	1.2	0.8	1.2	1.2
Input Freq. (MHz)	4	4	10	10	20
Total Power (µW)	83.8	231	202	526	1149
SNDR (dB)	57.62	59.63	53.27	55.70	49.46
SFDR (dB)	76.1	76.8	74.1	78.6	62.1
FOM (fJ/CS)	16.8	36.8	26.8	52.8	117
Technology	0.13µ	0.13µ	0.13µ	0.13µ	0.13µ
SAR Area (mm²)	0.056	0.056	0.056	0.056	0.056

VIII. References

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