Class A+ Amplifier with Controlled Positive Feedback for Discrete-Time Signal Processing Circuits

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***Abstract*— This paper demonstrates Class-A+ amplifier as an alternative to Class-A amplifier for discrete-time signal processing circuits. Class-A+ amplifier uses cross-coupled latches during the amplification phase at the output to improve settling accuracy compared to Class-A amplifier. The positive feedback latch is reset to fixed bias voltages of the Class-A output stage during the reset-phase. This dynamic compensation technique for realizing stable amplifier enables power and area savings with improved settling accuracy and THD performance. Simulation results show 30% reduction in overall power consumption, 50% reduction in the size of output stage and 10 dB improvement in settling accuracy compared to conventional Class-A amplifier with similar worst case settling time.**

I. INTRODUCTION

The various amplifier architectures shown in Fig.1 are optimized for speed, power, accuracy, signal swing, distortion and area for a given application [1]. The inter-dependant relationship of the above parameters leads to an inefficient design of the amplifier. In this paper, we demonstrate a controlled positive feedback approach for the output stage of the two-stage amplifier to relax the dependency on speed, area and power requirements suitable for switched-capacitor amplifier design. The paper is organized as follows. Section II briefly describes the architectures in Fig.1 and motivation for Class-A+ amplifier. In Section III Class-A+ amplifier details are given. Simulation results are presented in Section IV and conclusion is provided in Section V.

II. AMPLIFIER ARCHITECTURES

The various amplifier architectures are shown in Fig.1. Class-A amplifiers are typically two-pole systems with the output stage contributing to the second non-dominant pole. The second-stage/output stage burns significant power set by the bandwidth requirements and settling accuracy of the application. Also, the maximum slew-rate is limited by the bias currents of the first and second stages. Class-A amplifiers offer superior distortion performance at the expense of large quiescent power consumption. Class-AB and Class-B amplifiers de-couple this slew-rate, peak current and the quiescent current constraint to achieve low power consumption. However, Class-AB and Class-B amplifier suffers from significant distortion. In-order to accommodate Class-AB amplifiers and still meet the bandwidth, distortion and settling accuracy of Class-A amplifier, Class-A+ amplifiers is proposed in the next section.

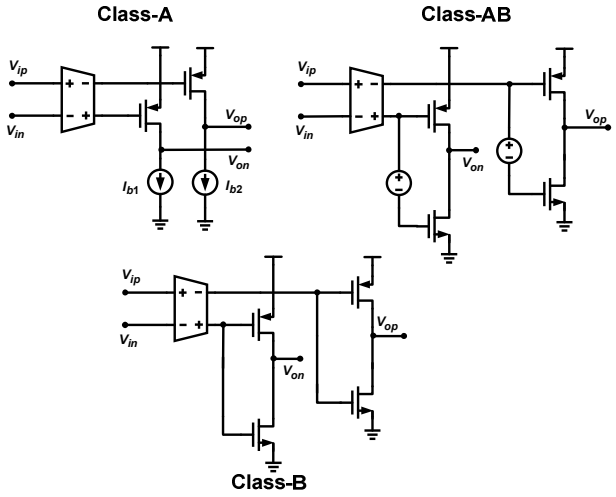

Fig.1. Amplifier Architectures

III. CLASS-A+ AMPLIFIER

The two-stage Class-A+ amplifier has the same first-stage as a conventional Class-A amplifier is shown in Fig. 2. By utilizing positive feedback, dynamic compensation is achieved for the output stage transconductance. This dynamic compensation for the amplifier relaxes area and power consumption with better settling accuracy and settling time.

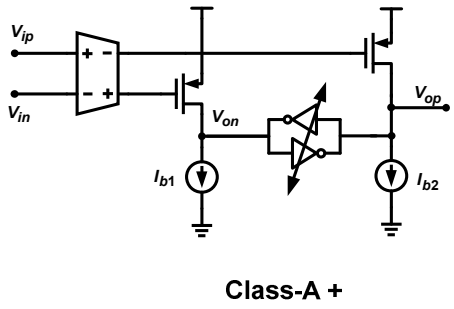

Fig.2. Class-A+ Amplifier

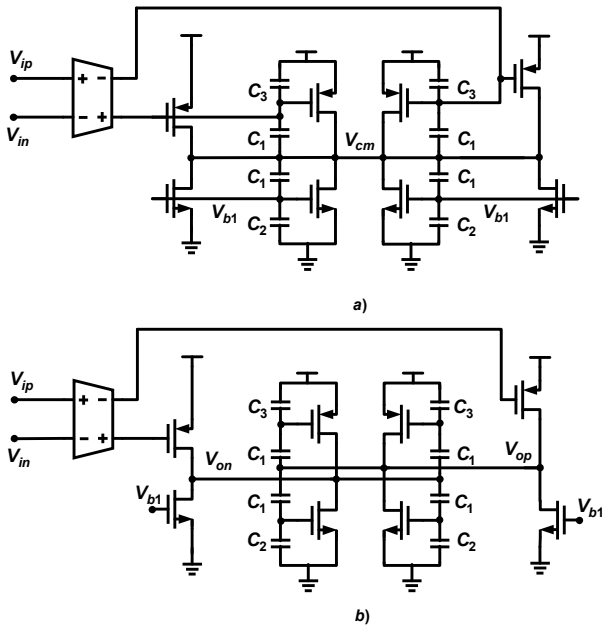

Fig.3. Class-A+ amplifier during a) reset phase and b) amplification phase

The reduction in the impedance of output stage and increase in the short-circuit transconductance of the output stage with the positive feedback latch is a design trade-off for a given settling accuracy [2]-[3]. The Class-A+ amplifier operates in two-phase and it is explained below.

In reset phase, the internal nodes of the latch are reset to known bias voltages of the Class-A amplifier as shown in Fig. 3a. In amplification phase, positive feedback is applied to the output stage as shown in Fig. 3b. The positive feedback ratio is set by the capacitor ratio (C_1,C_2,C_3) of the cross-coupled latch. The small signal model shown in Fig. 4 for the conventional miller/current buffer compensation is used to show the effect of positive feedback. The positive feedback increases the output stage short-circuit transconductance and decreases output stage impedance for miller compensated (MC) and current buffer (CB) based compensated amplifiers.

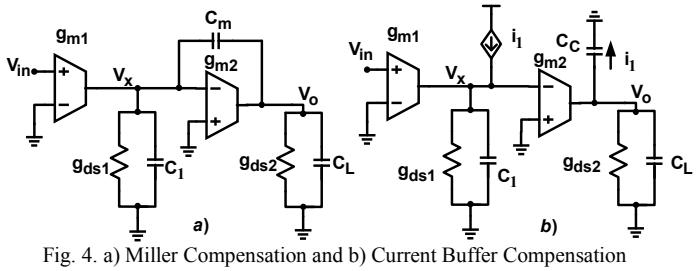

Fig. 4. a) Miller Compensation and b) Current Buffer Compensation

TABLE I MILLER COMPENSATED AMPLIFIER POLES

Amplifier	Miller Compensated Amplifier
Pole-1	$-\frac{g_{ds1}g_{ds2}(v_o)}{C_Lg_{ds1}+C_1g_{ds2}(v_o)+C_m(g_{ds1}+g_{ds2}(v_o)+g_{m2}(v_o))}$
Pole-2	$-\frac{C_Lg_{ds1}+C_1g_{ds2}(v_o)+C_m(g_{ds1}+g_{ds2}(v_o)+g_{m2}(v_o))}{C_1C_L+C_mC_L+C_mC_1}$
DC-Gain	$\frac{g_{m1}g_{m2}(v_o)}{g_{ds1}g_{ds2}(v_o)}$

The open-loop transfer function for the above amplifiers is shown in (1) and (2). The effect of positive feedback on poles of the above amplifiers is shown in TABLE I and II as functions of output voltage. Fig. 5 shows the location of open loop poles of a typical two-stage Class-A amplifier and Class-A+ amplifier at the beginning of amplification phase. The non-dominant output pole of the Class-A+ amplifier is moved to higher frequency with the help of positive feedback latch.

TABLE II CURRENT BUFFER COMPENSATION AMPLIFIER POLES

Amplifier	Current Buffer Compensated Amplifier
Pole-1	$-\frac{g_{ds1}g_{ds2}(v_o)}{C_Lg_{ds1}+C_1g_{ds2}(v_o)+C_C(g_{ds1}+g_{m2}(v_o))}$
Pole-2	$-\frac{C_Lg_{ds1}+C_1g_{ds2}(v_o)+C_C(g_{ds1}+g_{m2}(v_o))}{C_1C_L+C_CC_1}$
DC-Gain	$\frac{g_{m1}g_{m2}(v_o)}{g_{ds1}g_{ds2}(v_o)}$

In a macro-model simulation, Class-A amplifier was modeled as a two-pole system with the non-dominant pole placed at the closed-loop bandwidth frequency with DC-gain of 1000 and feedback factor of 0.5 [1]. Class-A+ amplifier was modeled as a two-pole amplifier with initial non-dominant pole at half the closed-loop bandwidth frequency whereas, DC-Gain and non-dominant pole vary with output swing.

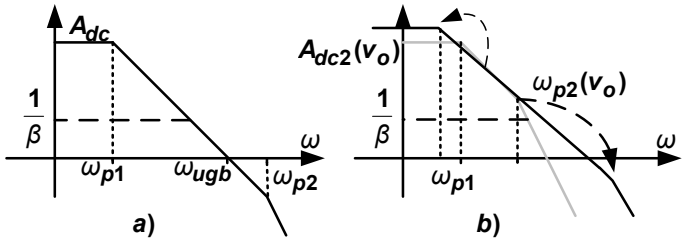

Fig. 5. a) Class-A open-loop poles and b) Class-A+ open loop poles during amplification phase

The simulation shows the step response of Class-A+ amplifier change from under-damped closed loop response at the beginning of the step response to improved dynamic and steady state settling accuracy at the end of amplification phase in Fig. 6.

$$\frac{V_o}{V_{in}} = -\frac{g_{m1}(g_{m2}-sC_m)}{s^2(C_1C_L+C_mC_L+C_mC_1)+s(C_Lg_{ds1}+C_1g_{ds2}+C_m(g_{ds1}+g_{ds2}+g_{m2}))+g_{ds1}g_{ds2}} \quad -(1)$$

$$\frac{V_o}{V_{in}} = -\frac{g_{m1}g_{m2}}{s^2(C_1C_L+C_cC_1)+s(C_Lg_{ds1}+C_1g_{ds2}+C_c(g_{ds1}+g_{m2}))+g_{ds1}g_{ds2}} \quad -(2)$$

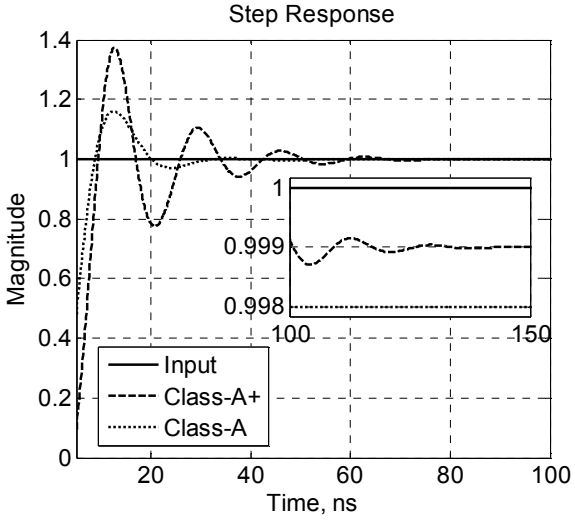

Fig. 6. Step Response

IV. SIMULATION RESULTS

This section compares Class-A+ amplifier against an over damped and an under-damped Class-A amplifier. The amplifiers were designed using 0.13 µm CMOS process with 1.2 V power supply. Cascode-compensation based Class-A amplifiers were used for the following comparison. Error amplifier based common-mode feedback was used for common-mode feedback. The above mentioned amplifiers were simulated in a sample and hold (S/H) configuration shown in Fig. 7. The S/H circuit was simulated with clock frequency of 20 MHz.

The Class-A amplifier has the best stability performance among the amplifiers in comparison. Class-A under damped amplifier has 50% reduced output stage devices compared to Class-A amplifier and hence degraded stability performance. Class-A+ amplifier was designed with 50% reduced output stage as compared to Class-A amplifier with cross-coupled latch. The differential stability of the amplifiers at the beginning of the amplification phase is listed in TABLE-III.

TABLE III. DIFFERENTIAL STABILITY ANALYSIS

Amplifier	Differential Stability Analysis	
	Phase Margin	*Phase Margin Frequency*
Class-A over-damped	74°	124 MHz
Class-A under-damped	55°	178 MHz
Class-A+	38°	155. 8 MHz

Step response of the amplifiers is shown in Fig. 8, steady-state setting error is shown in Fig. 9 and 0.1% settling time is shown in Fig. 10. The step-response clearly shows the dynamic nature of Class-A+ amplifier. In the beginning of amplification phase, the Class-A+ amplifier behaves closer to under-damped Class-A amplifier. The positive feedback improves stability and DC-gain of the amplifier.

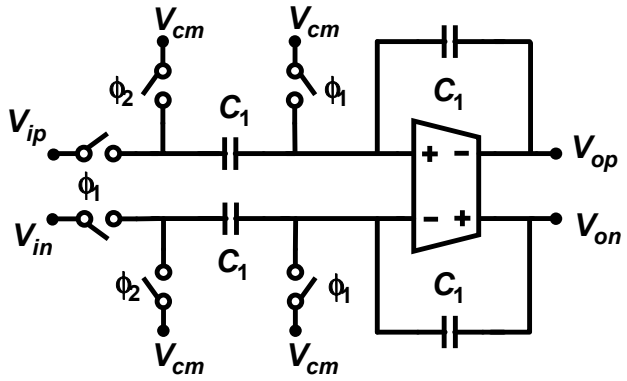

Fig. 7. S/H Simulation Setup

Settling accuracy is better than Class-A amplifier at the end of amplification phase. Better settling accuracy is achieved with 30% less quiescent current and 50% reduction in the output stage as compared to over damped Class-A amplifier design. Since the positive feedback is output signal dependant, settling accuracy for a given settling time was verified across the input signal range. Fig. 9 shows % settling error across the entire input range. Class-A+ amplifier has better than 10-dB improvement in steady state settling accuracy. Steady state settling accuracy is improved due to the increase in loop gain by positive feedback latch.

Similar worst case 0.1% settling time as compared to Class-A amplifier is shown in Fig. 10. Total-harmonic distortion of over-damped Class-A amplifier and Class-A+ amplifier is shown in Fig. 11. The Class-A+ amplifier has better than 3 dB THD as compared to Class-A amplifier across the input frequency range. The SFDR performance of Class-A+ amplifier is better than 6 dB as compared to Class-A amplifier.

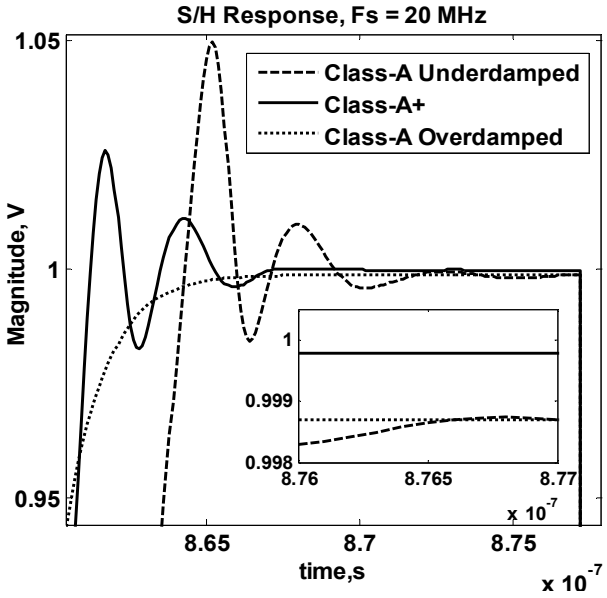

Fig. 8. S/H Response with unit step input

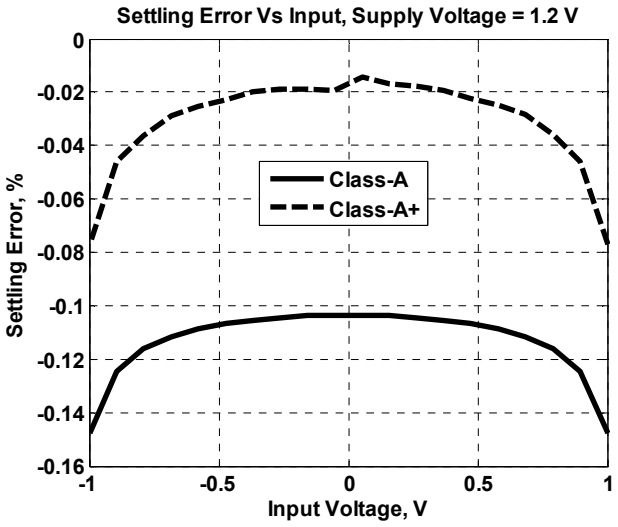

Fig. 9. Settling Error % Vs Input

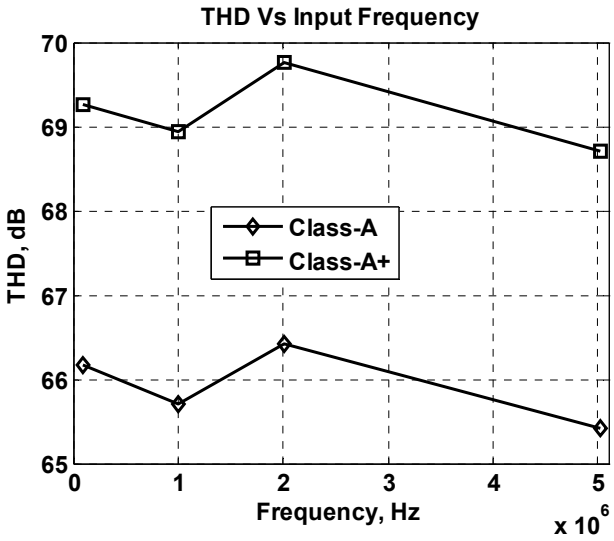

Fig. 11. THD Vs Input Frequency, Class-A and Class-A+ amplifier

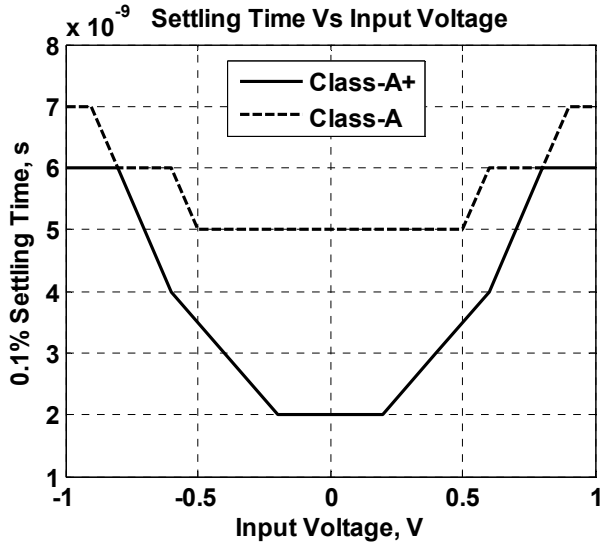

Fig. 10. 0.1% Settling time Vs Input Voltage

V. CONCLUSION

Class-A+ amplifier is suited for discrete time signal processing circuits. The Class-A+ amplifier utilizes controlled positive feedback for the output-stage transconductance to improve settling accuracy with power and area savings as compared to Class-A amplifiers. This leads to 30% reduction in overall power consumption, 50% reduction in output-stage area and 10 dB improvement in settling accuracy with similar worst case settling time. The amount of positive feedback, settling accuracy and reduction in output stage power/area is a design trade-off for a given application such as Switched-capacitor filters or Data-Converters.

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