Enhanced SAR ADC Energy Efficiency from the Early Reset Merged Capacitor Switching Algorithm

Jon Guerber, Hariprasath Venkatram, Taehwan Oh, Un-Ku Moon
Department of Electrical Engineering and Computer Science, Oregon State University
Corvallis, Oregon, USA
[guerberj@lifetime.oregonstate.edu]

***Abstract*—The early reset merged capacitor switching algorithm (EMCS) is proposed as an energy reducing switching technique for a binary weighted, capacitive successive approximation (SAR) analog to digital converter (ADC). The method uses the merged capacitor switching (MCS) architecture and optimizes the use of the V_{CM} level during the SAR conversion. This algorithm can reduce switching power by over 12% with no additional DAC driver activity when compared to the MCS scheme. The MCS and EMCS approaches are analyzed mathematically and the EMCS energy consumption is shown to be lower than or equal to that of the MCS technique for every digital code. Static linearity improvements for this structure are also shown with the integral non-linearity (INL) reducing by a factor of two due to the utilization of the MCS three level DAC. The EMCS implementation methodology is also described.**

I. Introduction

Power efficiency in data conversion has become an increasingly demanded requirement with the introduction of mobile devices, implantable electronics, and energy harvesting sensor networks. While this power requirement has been met in digital circuits with smaller process technology nodes, the benefit does not easily translate to many traditional analog to digital converter (ADC) structures due to the need for accurate amplification or integration. Today, for medium resolution and sampling rate applications, the successive approximation (SAR) ADC has become popular due to its increased digital nature, reduced analog complexity, and intrinsically low power consumption.

While generic SAR structures have low power consumption, a desire to further reduce losses, motivated by both consumer and industrial needs, has led designers to analyze SAR block level efficiency and find ways to mitigate wasted energy. For the traditional binary capacitor based SAR without calibration, the capacitor array can often consume a large fraction of the total power consumption. Careful study has shown that the switching algorithms employed by SAR converters can have dramatic effects on the losses through this capacitor bank. It has been demonstrated in [1] that by splitting the MSB capacitor into sub-capacitors the switching power can be reduced by 37% over the traditional approach [2], while the "monotonic" method demonstrated an 81% improvement by switching only one side of a differential capacitor array per bit [3]. The merged capacitor switching (MCS) algorithm of [4]-[5] improves this savings to 87.5% by utilizing the common mode reference already present in a differential SAR. This paper will show that the MCS switching efficiency and static linearity are further improved by intelligently selecting the time that individual binary capacitors are reset with the early reset MCS (EMCS) algorithm. Section II of this paper will analyze the MCS algorithm and Section III will identify MCS in-efficiencies and propose the optimized EMCS methodology. Section IV will describe the implementation and effect on other SAR circuit components with conclusions discussed in section V.

This work was funded in part by Texas Instruments and the Center for the Design of Analog-Digital Integrated Circuits (CDADIC)

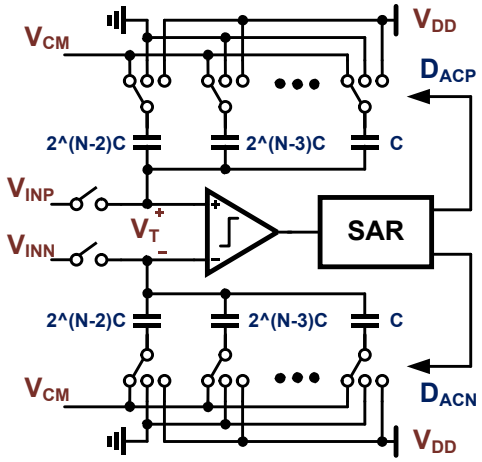

Fig. 1. Merged capacitor switching (MCS) SAR architecture

II. The Merged Capacitor Switching (MCS) SAR

While many SAR switching algorithms exist for un-calibrated binary weighted capacitive structures, the merged capacitor switching algorithm [4] (also known as common mode based charge recovery [5]) has been shown to be the most energy efficient to date. The operation of the MCS SAR begins by sampling the differential input signal onto the virtual ground nodes of the SAR with the back end of the capacitor bank tied to V_{CM} as shown in Fig. 1. With the input voltage sampled, the polarity of the input is first determined with the single comparator. This information is stored in the SAR registers and the DAC will subtract or add a differential voltage from the virtual ground nodes based on this polarity. If the comparator output is a 1, V_{DD} and G_{ND} will switch to the bottom plate of the positive and negative MSB capacitors respectively, subtracting $V_{DD}/4$ from the differential input. If the comparator code is 0, the V_{DD} and G_{ND} will switch to the bottom plate of the negative and positive MSB capacitor respectively, differentially adding $V_{DD}/4$. Further cycles will add or subtract in the same manner with the DAC weight

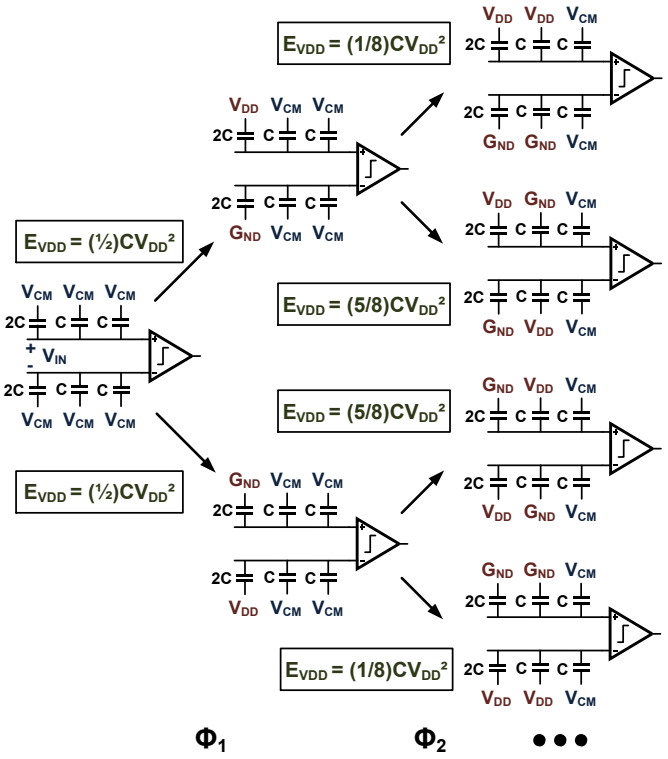

Fig. 2. MCS SAR switching diagram and supply energy for a 3b example

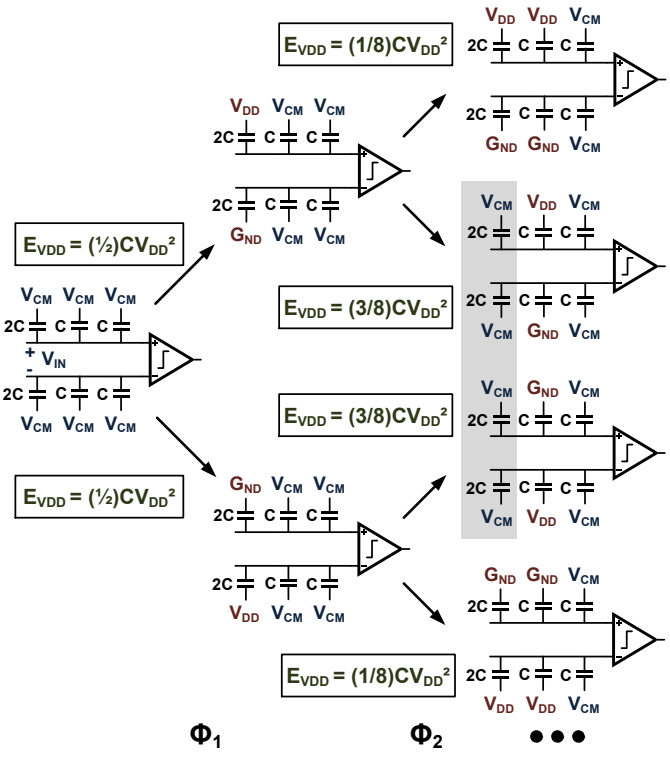

Fig. 3. EMCS SAR switching diagram and supply energy for a 3b example

decreasing by a factor of 2 in each cycle. This switching method achieves low power consumption given that there is only one switching event per bit, the back side capacitor voltage is centered at the common mode, and the first bit is determined before any DAC operations. Furthermore, this switching still allows the virtual ground common mode of the SAR to be constant with no net power drawn from V_{CM}, even during the reset phase.

The energy per code of the MCS switching scheme can be quantified by first examining the DAC power required in an example 3-bit MCS SAR. Fig. 2 shows this example 4C total capacitance MCS SAR and the energy required for each operation based on the current and previous codes. Here, in the first cycle, switching charge derived from V_{DD} can be determined by calculating the differential voltage on the MSB capacitor (shown in equation 1 as the bottom plate voltage increase minus the top plate voltage increase) and multiplying by the switched capacitance. The cycle energy can then be found by multiplying the switching charge with the supply as shown:

$$\phi_1 :\ E_{VDD} = \left[\left(\frac{1}{2} - \frac{C_{MSB}}{2C_T}\right)V_{DD}C_{MSB}\right]V_{DD} = \frac{C_{Unit}{V_{DD}}^2}{2} \quad (1)$$

Where C_{UNIT} is defined as the LSB capacitor and the larger capacitors are composed of multiples of C_{UNIT}.

The energy from V_{DD} of the second transition can be found in the same way for the second capacitor; however since the virtual group voltage is moving with respect to the MSB capacitor, another term will need to be included. When the virtual ground voltages moves with respect to a V_{DD} referenced capacitor, additional charge will be added or subtracted from the supply as shown:

$$\begin{aligned}\phi_2 : E_{VDD} &= \left[\left(\frac{1}{2} - \frac{C_{MSB-1}}{2C_T}\right)V_{DD}C_{MSB-1}\right]V_{DD} + C_{VDD}\left(\frac{C_{MSB-1}}{2C_T}\right){V_{DD}}^2 \\ &= \frac{5C_{Unit}{V_{DD}}^2}{8}\end{aligned} \quad (2)$$

One can observe from equation 2 that there is an energy efficient switching step if the stage digital bit is the same as the previous bit and the step is less efficient if the bits are of the opposite polarity because of the previously switched capacitors connected to V_{DD}. The total power of a given cycle (other than the MSB) can be generalized as the following:

$$\begin{aligned}\phi_N :\ E_{VDD} &= \left[\sum_{S=1}^{N-1} C_S\left(b_N \oplus b_S\right)\right]\left(0 + \frac{C_N}{2C_T}\right){V_{DD}}^2 \\ &+ \left[\sum_{S=1}^{N-1} C_S\overline{\left(b_N \oplus b_S\right)}\right]\left(0 - \frac{C_N}{2C_T}\right){V_{DD}}^2 \\ &+ \left(\frac{1}{2} - \frac{C_N}{2C_T}\right){V_{DD}}^2 C_N \\ &= \frac{C_N{V_{DD}}^2}{2C_T}\left[\sum_{S=1}^{N-1} C_S\left(-1\right)^{\overline{\left(b_N \oplus b_S\right)}} - C_N + C_T\right]\end{aligned} \quad (3)$$

Where N is the given stage and ($b_N \oplus b_S$) is the XOR of the current bit (b_N) and the previous stage bit (b_S). The total energy of a given MCS SAR conversion is then given by:

$$E_{VDD}(Code) = \frac{{V_{DD}}^2}{2C_T}\left[\sum_{N=1}^{M-1} C_N\left(\left(\sum_{S=1}^{N-1} C_S(-1)^{\overline{(b_N \oplus b_S)}}\right) - C_N + C_T\right)\right] \quad (4)$$

Where M is the SAR ADC resolution in bits and {b_1, … b_N} is the digital representation of the given code.

III. Early Reset MCS SAR

Looking at the MCS SAR described in section II, one can see that in the second cycle, switching in the same direction as the previous cycle results in significantly less energy than switching in the opposite direction. However, switching in the opposite direction to correct a previous virtual ground overshoot is not always the only available option to generate the needed virtual ground voltage. Another solution is to reset the previous capacitor to V_{CM} and switch the current capacitor to the opposite polarity as shown in Fig. 3. By doing this, the energy for the capacitance connected to V_{DD} is reduced since the total supply referenced capacitance is decreased before the virtual ground node voltage changes and extra charge is added from the supply. This energy in the second phase for this {1,0} transition is given as the following:

$$\phi_2 : E_{VDD} = \left[\left(\frac{1}{2} - \frac{C_{MSB-1}}{2C_T}\right) V_{DD} C_{MSB-1}\right] V_{DD} = \frac{3C_{Unit}{V_{DD}}^2}{8} \quad (5)$$

Switching the previous capacitor to V_{CM} requires no additional energy since it would be switched during the reset phase and any prior charge on the capacitors is differential and canceled across the shared V_{CM} node. Furthermore, reducing the supply referenced capacitance in early stages will also continue to reduce energy due to virtual ground movement in later stages. The function of the early reset MCS (EMCS) SAR algorithm is thus to reset the previous capacitor and charge the current capacitor in a given DAC operation to the opposite charge if the current bit is the opposite polarity of the previous bit. This results in the maximum energy efficiency for a 3-level DAC SAR.

When comparing the energy of the MCS and EMCS techniques, the main difference of the EMCS algorithm is that capacitors for a given bit are only held at VDD and GND if, in the corresponding MCS digital code, the previous and next bits are the same. As an example, if the MCS digital code was {1,1,0} we know that in the second cycle the MSB-1 capacitor is charged to a "1' state. However since the next bit is a zero, the MSB-1 capacitor is reset in the next phase to V_{CM} while the MSB-2 capacitor is charged to a "1" state. In the {1,0,0} code the MSB-1 capacitor is charged to a "1" in the second stage and reset to V_{CM} in the third stage since the new {V_{CM}, 1, 0} has an alternating second and third bit. Therefore, for any binary digital code representation, the supply connected capacitance corresponding to a given bit is dependent only on the previous and next bits being different. We can quantify the energy per stage of the non-MSB EMCS SAR cycles with codes corresponding to a typical binary representation as shown with the following:

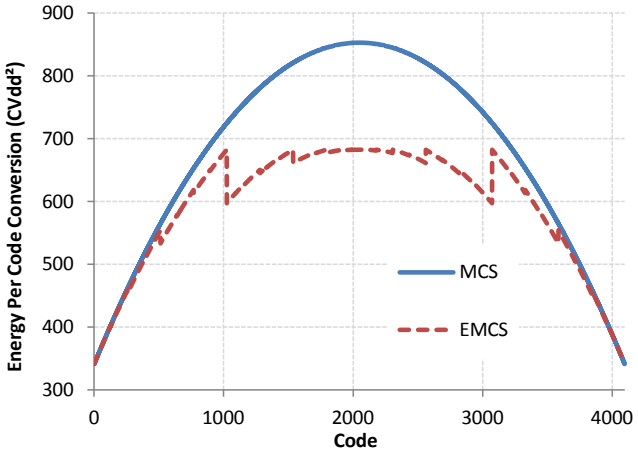

Fig. 4. SAR switching energy per code for the MCS and EMCS structures in a 12b ADC.

$$\phi_N : E_{VDD} = \frac{C_N {V_{DD}}^2}{2C_T}\left[\sum_{S=2}^{N-1}\left(C_S\overline{(b_{S-1} \oplus b_{S+1})}(-1)^{\overline{(b_N \oplus b_{S+1})}}\right) + C_1\overline{(b_1 \oplus b_2)}(-1)^{\overline{(b_N \oplus b_1)}} - C_N + C_T\right] \quad (6)$$

The EMCS energy per binary digital code is then given by:

$$E_{VDD}(Code) = \frac{{V_{DD}}^2}{2C_T}\left(\sum_{N=1}^{M-1} C_N\left[\sum_{S=2}^{N-1}\left(C_S\overline{(b_{S-1} \oplus b_{S+1})}(-1)^{\overline{(b_N \oplus b_{S+1})}}\right) + C_1\overline{(b_1 \oplus b_2)}(-1)^{\overline{(b_N \oplus b_1)}} - C_N + C_T\right]\right) \quad (7)$$

By comparing the power dissipation of the MCS and EMCS SARs, we can see that for every possible code, the EMCS SAR has equal or lower energy:

$$E_{VDD,MCS}(Code) \geq E_{VDD,EMCS}(Code)$$

$$\sum_{S=1}^{N-1} C_S(-1)^{\overline{(b_N \oplus b_S)}} \geq \left[\sum_{S=2}^{N-1}\left(C_S\overline{(b_{S-1} \oplus b_{S+1})}(-1)^{\overline{(b_N \oplus b_{S+1})}}\right) + C_1\overline{(b_1 \oplus b_2)}(-1)^{\overline{(b_N \oplus b_1)}}\right] \quad (8)$$

The energy per code is also plotted in Fig. 4 for a 12b SAR operation normalized to (C_{UNIT}*${V_{DD}}^2$) and energy reduction can be seen for each code. For a uniform input probability density function (PDF), the EMCS structure results in 12.5% lower average switching energy and an even lower 18.4% when the input has a Gaussian distribution (since the Gaussian PDF has more codes in the EMCS reduced energy region). The switching energy is lower for central codes since the EMCS greatly reduces the power of alternating codes that would be seen in an MCS configuration. Compared to the set and down technique [3], the EMCS technique provides a 41.5% average switching energy reduction.

Finally, the worst case code for the ADC differential non-linearity (DNL) is now no longer {1,0,0,0…} to {0,1,1,1…} since this code has an alternating set of bits. Rather the worst case transitions are now from {1,V_{CM}, V_{CM}, V_{CM}…} to {V_{CM}, 1, 1, 1…} and {0,V_{CM}, V_{CM}, V_{CM}…} to {V_{CM}, 0, 0, 0…}.

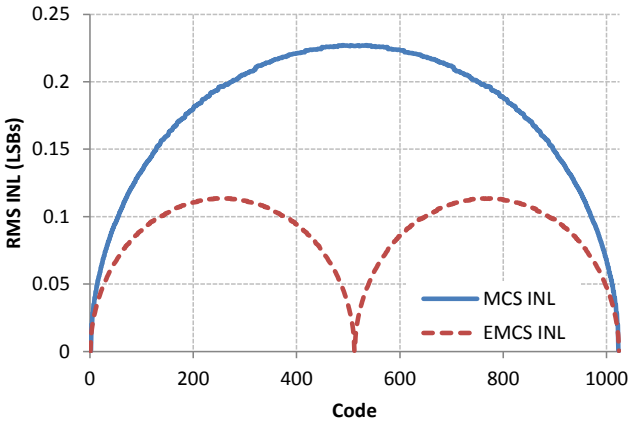

Fig. 5. RMS INL in LSBs for the MCS and EMCS 10b SAR ADC structures with a unit capacitor sigma of 0.02 LSB (10,000 simulations) [7]

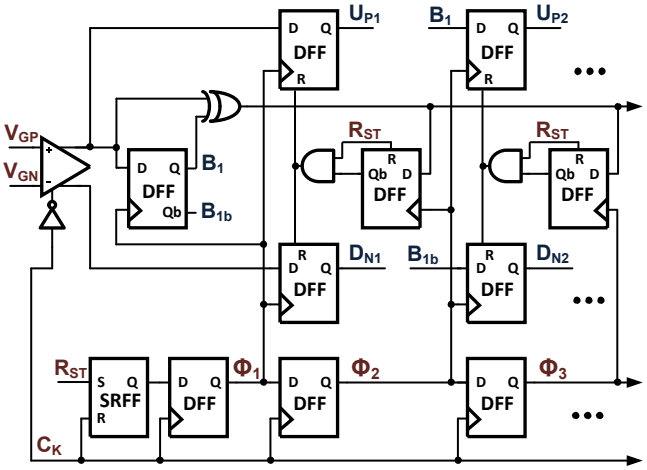

Fig. 6. Sample logic implementation for the EMCS SAR ADC

Here, the effective variance of the virtual ground charge due to the worst case code capacitor matching requirement is reduced by a factor of 2 over the MCS SAR variance meaning the DNL is reduced by a factor of two on average. The integral non-linearity (INL) is also reduced by a factor of two as shown in Fig. 5, and exhibits a dual lobe behavior due to the presence of the all "V_{CM}" code which codes all capacitors with one value just like an all "1" or "0" code.

IV. EMCS Implementation

The EMCS structure achieves a greater switching power efficiency and static linearity by identifying whether a current bit is the same as the initial first comparison output. If it is the same, the first comparator decision is kept and sent to the DAC. If the bit is complementary to the initial, the previous DAC value is reset to V_{CM}.

Typically in a SAR register block, the output of the comparator is captured onto a flip flop which is clocked by the appropriate SAR phase generated by a state machine. Due to the EMCS algorithm however, one can see that the current bit is always the same as the first bit regardless of the comparator output. At the circuit level, the comparator will only give information as to whether or not the previous bit should be reset to V_{CM}. Because of this operation, the EMCS structure is the same as in Fig. 1, with the only change being the SAR logic, which can be modified as shown in Fig. 6 with the addition of only a few extra gates. Here, the MCS configuration consisting of positive and negative flip flop registers are employed and when neither flip flop is holding a 1, the corresponding DAC capacitor is tied to V_{CM}. In the EMCS structure however, if the comparator output is different than the first bit, that previous stage's flip flops are synchronously reset and the current flip flop output is a copy of the previous. The final data output is then valid and has a modified three-level coding (GND, V_{CM}, V_{DD}) which can be easily added to return to a binary representation. This switching method does not add any extra activity or loading to the DAC capacitor drivers since all capacitors would need to be reset anyway before sampling the next analog input. It should also be noted that most SAR architectural variations building upon the MCS switching structure, such as the ternary SAR [6], can still reap greater energy savings with an EMCS switching algorithm. Finally, EMCS transistor level simulations in 0.13µm CMOS have been performed and show about a 10% switching power reduction (lowered due to capacitive parasitics) for a 10b SAR over the MCS structure.

V. Conclusion

This paper has analyzed the merged capacitor switching algorithm and proposed the early reset MCS switching technique to further reduce switching power consumption by over 12% and improve static linearity by a factor of 2 over the MCS SAR ADC. This method better utilizes the available common mode reference in the MCS DAC and is shown to improve or match energy efficiency for every code. The implementation can be made with little logic overhead and does not increase DAC driver power.

VI. Acknowledgment

The authors would like to thank Manideep Gande for his insightful discussions and the anonymous reviews for their helpful comments.

References

[1] B. Ginsburg and A. Chandrakasen, "An energy efficent charge recycling approach for a SAR converter with capacative DAC," *Proc. of IEEE Int. Sym. On Circuits and Systems*, ISCAS, pp. 184-187, 2005.

[2] J. McCreary, and P. Gray, "All-MOS charge redistribution analog-to-digital conversion techniques-part I," *IEEE J. Solid-State Circuits*, vol. SC-10, no. 6, pp. 371-379, Dec. 1975.

[3] C. Liu, S. Chang, G. Huang, and Y. Lin, "A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 731-740, Apr. 2010.

[4] V. Hariprasath, J. Guerber, S.-H. Lee, U. Moon, "Merged capacitor switching based SAR ADC with highest switching energy-efficnecy," *Electron. Lett*., vol. 46, pp. 620-621, Apr. 2010.

[5] Y. Zhu, C.-H. Chan, U. Cho, S.-W. Sin, S.-P. U, R. Martins, F. Maloberti, "A 10-bit 100-MS/s reference-free SAR ADC in 90nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1111-1120, Jun. 2010.

[6] J. Guerber, M. Gande, H. Venkatram, A. Waters, and U. Moon, "A 10b ternary SAR ADC with decision time quantization based redundency," Proc. *IEEE Asian Solid-State Circuits Conf.,* pp. 63-65, Nov. 2011.

[7] C. Lin, and K. Bult, "A 10-b, 500MSample/s CMOS DAC in 0.6mm^2," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 1948-1958, Dec. 1998.