Correlated Jitter Sampling for Jitter Cancellation in Pipelined TDC

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***Abstract*—In this paper, the Correlated Jitter Sampling (CJS) technique, which alleviates the jitter induced error from the time reference in pipelined Time-to-Digital Converter (TDC), is proposed. The auxiliary pipelined TDC is employed to remove the jitter induced error of the main pipelined TDC in the CJS technique. A 12b pipelined TDC adopting the CJS technique in the 1st time quantization stage is simulated to validate the proposed technique. Simulation results show that the TDC can achieve a flat SNDR performance of 70dB regardless of the jitter from time reference up to 25% jitter of $1T_{LSB}$ in reference clock, which is the maximum error allowed within a designed redundancy range of the pipelined TDC.**

I. INTRODUCTION

Time domain quantization is commonly used in many applications such as time of flight measurement, laser range finders, and phase measurement of digital PLLs. Also the power efficiency for the quantization can be improved with the aggressive scaling of recent CMOS process [1], [2]. However, it is not easy to achieve high resolution in TDCs due to the difficulty of linear time amplification without calibration [3], [4]. To increase the time resolution of the TDC, a simple time amplification method which adopts different slopes for charging or discharging with different current ratio can be used [5], [6]. With time amplification, the pipelining of the time quantization similar to the pipelined analog-to-digital conversion can be possible for further increase of time resolution.

Fig. 1 shows one possible example of a time pipeline stage for the pipelined TDC. It consists of a sub-TDC for quantization and other blocks for time residue generation. After the reset phase, the time input (T_{IN}) is quantized by the sub-TDC which generates the digital output and DAC pulse (T_{DAC}) for residue generation. As shown in Fig. 2, T_{DAC} is generated according to T_{IN} from the time reference (T_{REF}) after quantization. Then, the time residue (T_{DAC}-T_{IN}) is amplified by 4 with a different current ratio of 4:1 for charging and discharging in this example. After the zero-crossing comparison, the time output (T_{OUT}) is generated for further quantization in next pipeline stage. With time residue

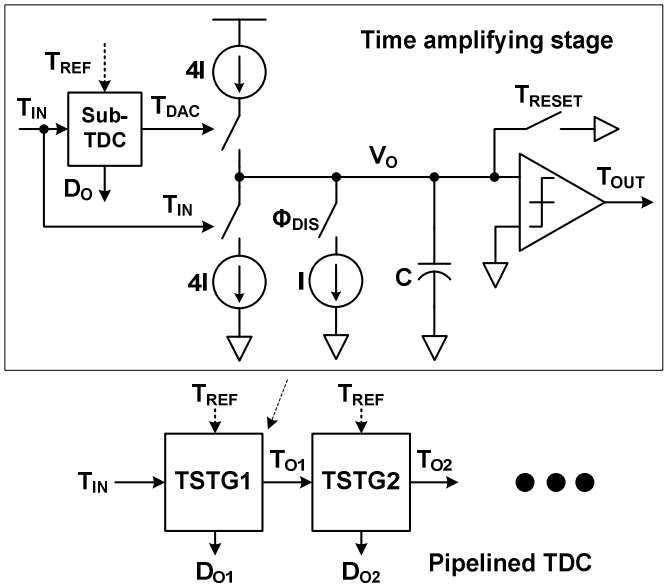

Fig. 1. Pipelined TDC example with time amplifying stage.

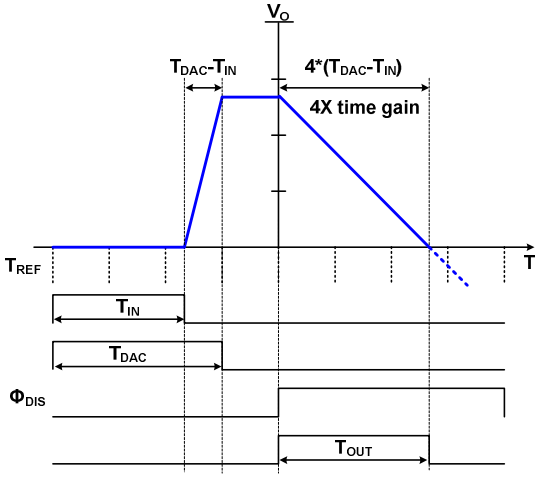

Fig. 2. Timing diagram of the time amplifying stage.

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amplification and its simple open loop configuration, this architecture is a good candidate for high resolution TDCs with relatively small power consumption. However, it also has many major error sources such as the nonlinearity of the current source, the noise of the comparator, and the jitter of the time reference. Although, other error sources can be treated as design trade-offs, the jitter of the time reference will directly limit the pipelined TDC performance for high SNR. In order to achieve N-bit SNR, the required jitter tolerance in the time reference is less than $1T_{LSB}$ of the N-bit TDC resolution, which is not easy to achieve in high resolution cases with fine time reference.

This paper presents the Correlated Jitter Sampling (CJS) technique which cancels the jitter induced error from the time reference in pipelined TDC. In section II, we will briefly review the background of the idea and explain the proposed technique. Simulation results and a conclusion will be followed in sections III and IV, respectively.

II. CORRELATED JITTER SAMPLING

A. Background

As a time reference for TDC, either a high frequency clock source or a voltage controlled delay line (VCDL) can be used [7]. The high frequency clock usually suffers from clock jitter and VCDL suffers from the mismatch of each delay unit to provide the fine time reference. One observation of the clock is shown in Fig. 3. By assuming a Gaussian distribution for clock jitter, the average period can be a fixed value ($T_{avg.}$) regardless of the clock phase because the jitter induced error can be averaged out. In the case of the VCDL, even with the averaging, the time reference still suffers from non-linearity due to static component mismatch. In the proposed technique, we utilize this characteristic of the clock to evaluate and cancel the jitter induced error.

B. Proposed CJS Technique

Fig. 4 shows the proposed CJS technique employed in the pipelined TDC. It consists of two pipelined TDCs and extra digital blocks for code averaging and subtraction. The time input (T_{IN}) is quantized by the main TDC based on the time amplifying stage as shown in Fig. 1. The time reference levels are provided from the clock signal. At the same time, the DAC pulse (T_{DAC1}) from the 1st stage of the main TDC (TSTG1) which has a jitter induced error from the time reference is also quantized in the auxiliary TDC. The key intent is for the auxiliary TDC has a same configuration as the main TDC except the 1st input stage (TINSTG) for T_{DAC1} input from the

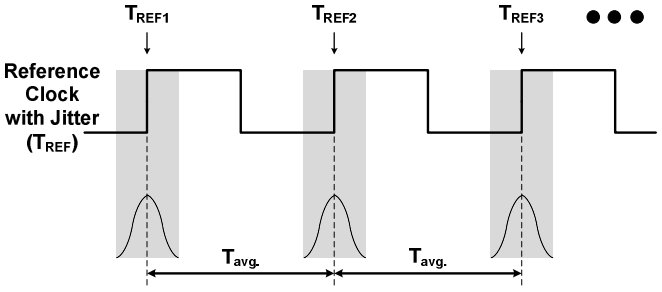

Fig. 3. Jitter observation of the clock reference.

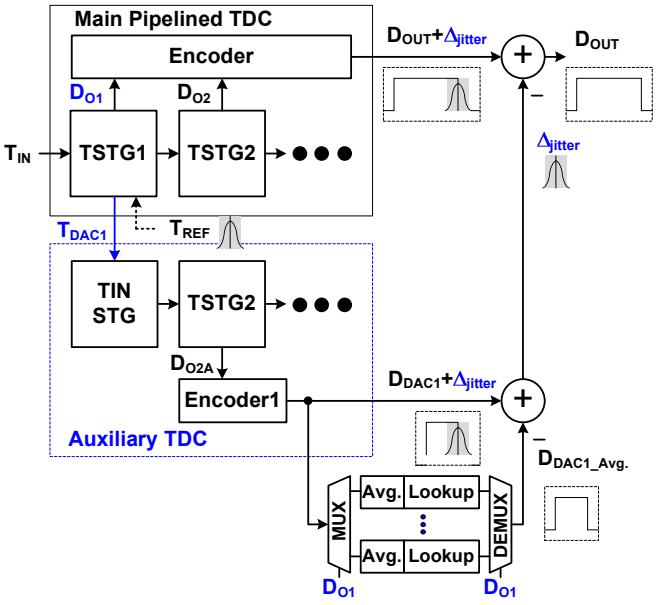

Fig. 4. Proposed correlated jitter sampling technique for pipelined TDC.

main TDC and extra digital blocks. Note that T_{DAC1} is the same pulse processed in the main TDC, which has the same information about the jitter from the reference clock. Now both main and auxiliary TDCs have the same jitter induced error (Δ_{jitter}) in their digital output. The output from the auxiliary TDC is then averaged in digital domain and stored in a lookup table depending on TSTG1 output (D_{O1}) for each DAC pulse.

After averaging, the lookup table has a set of ideal codes corresponding to each DAC pulse for the entire signal range, which can be used to extract the jitter information from the auxiliary TDC output. By subtracting the averaged DAC code in the lookup table from the auxiliary TDC output, we can now extract the code difference (Δ_{jitter}) between the DAC code with jitter induced error and the averaged DAC code. This code difference is further used to cancel the actual jitter in the main TDC to get the final output, D_{OUT}. Even though CJS in Fig. 4 only corrects the jitter induced error in the 1st stage, it can be extended to correct errors in more stages with additional auxiliary TDCs.

C. A Input Stage of Auxiliary TDC

Basic requirement of the CJS technique is that the jitter in both TDCs should be quantized with a same path gain for proper cancellation. It means the slopes for charging and discharging in both TDCs should be same. One problem arising from the proposed technique is the time difference required for discharging between the main and the auxiliary TDC paths. In the main TDC path, the residue time (T_{DAC1}-T_{IN}) is amplified with residue gain. As shown in Fig. 5 with a 4X residue gain, the maximum residue input to amplify in the main TDC path is $1T_{LSB}$, which generates $4T_{LSB}$ time output after residue amplification. However in the auxiliary TDC path, the maximum input from TDAC1 is $4T_{LSB}$. Thus the output of the auxiliary TDC path can be $16T_{LSB}$, which means 4X more time for discharging in auxiliary path to get the same path gain. One simple way to solve this problem is to use 1X

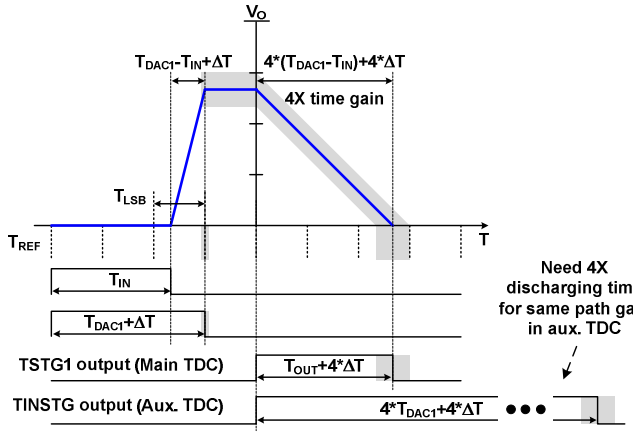

Fig. 5. Time output comparison for jitter induced error of main TDC and aux. TDC.

gain in the auxiliary TDC input path. The gain difference can be compensated by a 4X multiplication in digital domain. However, this method needs more accurate time resolution in the auxiliary TDC to get the same accuracy, after the digital domain multiplication.

Another solution is shown in Fig. 6. The basic idea is to reset the capacitor for charging to the different reference voltage depending on the DAC pulse, while using same slopes for charging and discharging during the same charging and discharging time in the auxiliary TDC path. It is equivalent to subtract the charge from the capacitor with a different voltage. Therefore, the stored charge on the capacitor for discharging is reduced in advance, resulting in the reduced discharging time of the auxiliary TDC path. Because we don't have the information about the DAC pulse from the main TDC before the charging is complete, parallel charging paths are employed to generate every possible residue. After the charging, the digital code from the 1st stage of the main TDC which has information about the DAC pulse, is used to select appropriate residue to discharge by the analog multiplexer. Because the auxiliary TDC only needs to provide the information about the code difference from the jitter, not the absolute code for DAC pulse itself, we don't need an accurate reset voltage for each capacitor reset in the 1st input stage of the auxiliary TDC. Therefore the design requirement for the reset voltage reference can be relaxed in the proposed input stage.

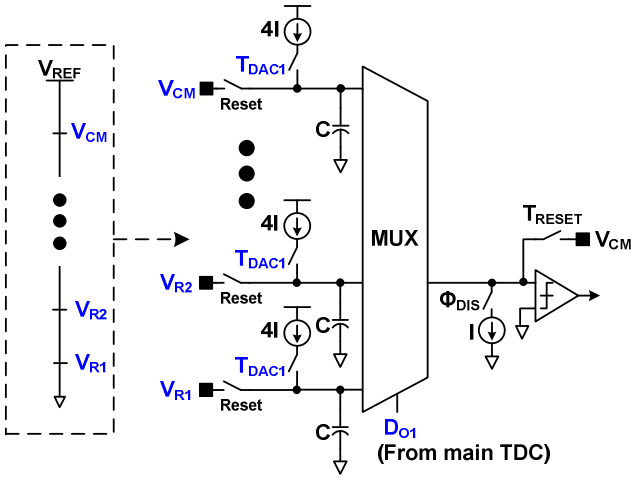

Fig. 6. Proposed input stage in auxiliary TDC for jitter measuring with same charging and discharging slope as in main TDC.

III. Simulation

To verify the CJS technique, a 12b pipelined main TDC and 10b pipelined auxiliary TDC models in Simulink are used for the simulation. 3b/stage architecture with 1b redundancy is employed in each pipeline stage model. In all simulations the time input of -1dBFS is applied. The simulated spectrum of TDC with the jitter in the reference clock is shown in Fig 7. Fig. 8 shows the SNDR comparison between with and without CJS technique for the different value of clock jitter. T_{LSB} is calculated for the time reference of the 1st stage with a sub-TDC resolution of 3b. Note that there is a 3dB drop from the ideal SNDR with CJS technique, which results from the additional quantization noise from the auxiliary TDC. Simulation shows that the jitter induced error can be canceled sufficiently with the proposed CJS technique, up to 25% RMS jitter of $1T_{LSB}$ in reference clock, which is the theoretical limit for the 3b/stage architecture with 1b redundancy. Due to the immunity to clock jitter with the proposed CJS technique, the design requirement of PLL can be relaxed significantly, if the PLL is used as a time reference. Fig. 9 and Fig.10 show the SNDR comparison versus the auxiliary TDC linearity and gain mismatch between TDCs, respectively, with 3% clock jitter. As shown in Fig. 9 and Fig. 10, the relaxed linearity and matching requirement enables to scale the auxiliary TDC path more aggressively than the accurate matching replica blocks of main TDC path.

IV. Conclusion

The Correlated Jitter Sampling (CJS) technique to cancel the jitter in pipelined TDC is proposed in this paper. With the proposed technique, the jitter induced error in the time reference can be corrected based on the information from the auxiliary TDC which measures the jitter error at the same time as the main TDC. Also the design requirement for the fine time reference to achieve the high resolution of TDC can be relaxed with the CJS technique.

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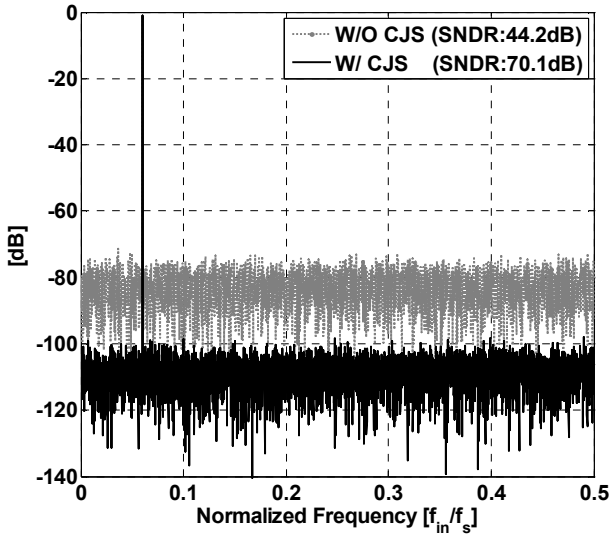

Fig. 7. Simulated TDC spectrum for 3% clock jitter.

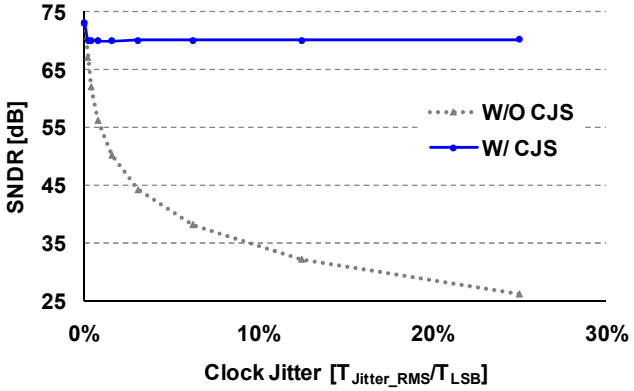

Fig. 8. Comparison of SNDR vs. jitter in clock reference.

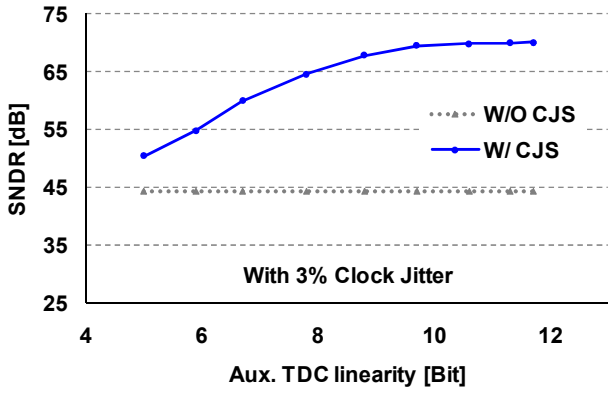

Fig. 9. Comparison of SNDR vs. Aux. TDC linearity for 3% clock jitter

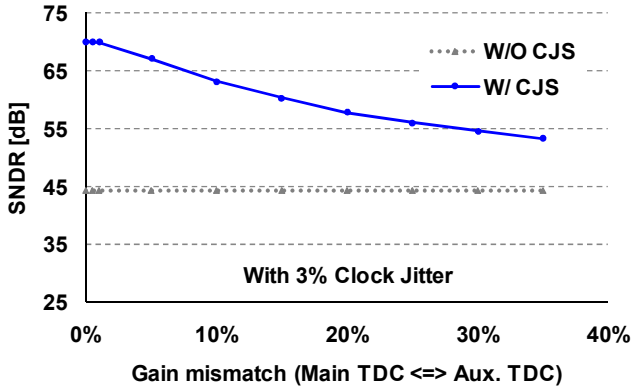

Fig. 10. Comparison of SNDR vs. gain mismatch between main TDC and aux. TDC for 3% clock jitter.