The Analysis and Application of Redundant Multistage ADC Resolution Improvements Through PDF Residue Shaping

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***Abstract*—An analysis of the statistics of multistage (pipeline, SAR, and algorithmic) ADCs with redundancy is performed and the ability to achieve an extra 6 dB of resolution in ADCs with half-bit redundancy is shown due to probability density function (PDF) residue shaping. This paper classifies redundancy techniques to show that only some have properties leading to statistical resolution improvements. When properly implemented, resolution gains are maintained even in the presence of large sub-ADC nonlinearity. ADC design criteria for maximizing these resolution increases through PDF residue shaping are described including improved back-end ADCs, stage comparator offset bounds, and the use of scaled conventional restoring with Z added levels (CRZ) stage redundancy. PDF residue shaped structural improvements are also quantified in relation to ideal and nonideal traditional multistage ADC structures.**

***Index Terms*—Algorithmic ADC, error correction, multistage ADC, pipeline redundancy, redundancy resolution improvement, residue shaping, SAR redundancy.**

I. Introduction

ROBUST, HIGH performance, and scalable analog to digital converters (ADCs) are critical for the operation of modern electronic devices in the field of communications, signal processing and sensor interfacing. ADCs in the 8–16 bit resolution range with bandwidths from 1–500 MHz are necessary for many applications such as video rate data conversion, communication receivers, medical instrumentation and modern telemetry. With the design of these ADCs come distinct tradeoffs between speed, power, resolution, and die area embodied within the many data conversion architectural variations [1], [2]. Making implementation choices has only become more difficult with the scaling of CMOS process technologies to meet digital density demands and the ever more stringent consumer requirements.

For medium to high resolution and bandwidth specifications, multistage ADCs such as pipeline, algorithmic, and SAR structures are often used to obtain the needed resolution with increased sample rate (pipeline), power (SAR), or area (algorithmic) benefits. These inherent structural advantages can be enhanced with the use of redundancy. Redundancy is the act of performing extra quantization on the input to an ADC stage, while maintaining the same overall ADC resolution, in order to achieve a greater tolerance to nonideal effects that cause over-range errors. This allows for the ability to compensate for settling errors [3]–[5], reduce the impact of comparator offsets [6], [7], allow for PN injectable background calibration [8]–[12], permit advanced correlated double sampling techniques to reduce amplifier gain requirements [13], and enhance the radiation hardening of critical high stress ADCs [14], [15]. Generally, the resulting benefits of redundancy include increased speed, reduced circuit power and complexity, and the ability to compensate for device and environmental mismatches.

The impetus for the use of redundancy is to tolerate small over-range errors caused by nonideal circuit behavior, and different types of redundancy implementations have been utilized over the past decades. It will be shown that the type of implementation can have varying effects on the statistics of the residue of each stage of a multistage ADC. This paper will analyze the statistical nature of the residue after each stage and demonstrate that for some quantization noise limited multilevel redundancy configurations, an extra 6 dB of resolution can be achieved. This resolution improvement will be shown to still be significant even in the presence of large comparator offsets or settling errors. Furthermore, design criteria for optimizing multistage ADCs for maximum resolution gain is discussed.

The paper is organized as follows. Section II will classify the various forms of multistage ADC redundancy based on statistical and implementations differences. Section III will analyze the probability density function (PDF) residue shaping of the multilevel redundancy and describe resolution benefits. Section IV will discuss PDF residue shaping in the context of circuit nonidealities and Section V will summarize the paper with design conclusions.

II. Multistage ADC Redundancy

While the various types of redundancy in multistage ADCs play the similar role of correcting over-range errors due to circuit and environmental nonidealities, they can be generally classified based on implementation and statistical behavior. In this paper, redundancy will be grouped into the four general categories of half-bit, conventional restoring with Z added levels (CRZ), sub-radix, and extra stage. There is of course categorical overlap in some modern redundancy schemes, but for simplicity only these four sets will be described. Also, only multistage ADC redundancy is considered here, not redundancy provided

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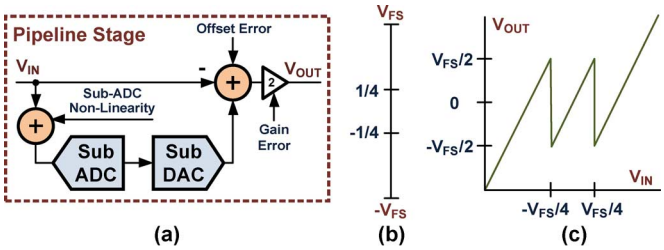

Fig. 1. 1.5b/stage pipeline ADC example with: (a) the pipeline stage block diagram; (b) sub-ADC 1.5b threshold levels; and (c) stage residue transfer curve.

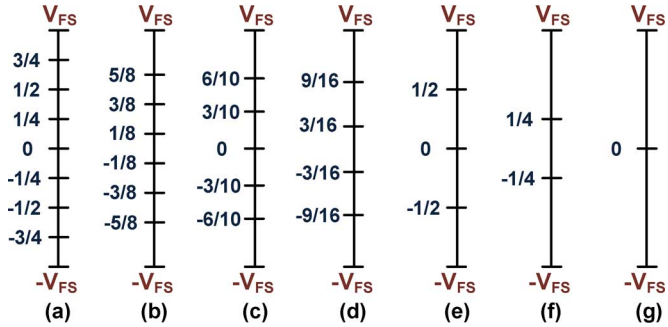

Fig. 2. Example low-resolution stage threshold levels. (a) 3b. (b) 2.5b. (c) $\mathrm{CRZ}_{\mathrm{Z}=2}$. (d) $\mathrm{CRZ}_{\mathrm{Z}=1}$. (e) 2b. (f) 1.5b. (g) 1b.

by system processing such as in some communication protocols [16].

A. Half-bit Redundancy

Half-bit redundancy is commonly found in pipeline and algorithmic ADCs but can also be present in SAR structures [17]. Historically, this redundancy was created to mitigate sub-ADC nonlinearity in pipeline stages [7] illustrated in Fig. 1(a). This was separately discovered for algorithmic ADCs in [18], [19] and is sometimes referred to as redundant signed digit (RSD) redundancy. The implementation of this redundancy conceptually consists of taking a given full-bit sub-ADC stage and replacing each given comparator level with two new comparison levels that closely surround the old comparison level. Ideally, these comparison levels should be located within 0 and $\mathrm{V_{LSB}}/2$ of the original threshold, when referenced to the sub-ADC resolution. By doing this, the ideal residue of each stage is now half of what it previously was and over-range errors between $\pm\mathrm{V_{FS}}$ and $\pm 3\mathrm{V_{FS}}/2$ of each stage are shifted back into the full-scale residue range after each cycle. Alternatively, half-bit redundancy can be understood as a shifting of the sub-ADC stage comparison thresholds, that is one bit higher resolution than is needed, by $\mathrm{V_{LSB}}/2$ and removing the top level [7]. The requirement that the sub-ADC levels now be accurate to within $\mathrm{V_{LSB}}/2$ ($\mathrm{V_{FS}}/4$ for a 1.5 b/stage ADC) of the current stage is a stark improvement to the traditional full-bit ADC structure which needs comparison levels that are accurate to within $\mathrm{V_{LSB}}/2$ of the entire ADC. For maximum offset tolerance of sub-ADC comparator offsets, the redundant comparison thresholds are often nominally placed at $\pm\mathrm{V_{LSB}}/4$ (of the current stage) away from the full-bit comparison thresholds.

Since these redundant sub-ADCs are not an integer number of bits, but can be added with 2 binary digits (three levels), they are often referred to as M.5 b/stage ADCs (1.5, 2.5, 3.5 etc.). Every M.5 b/stage redundant ADC contains $(2^{(\mathrm{M}+1)}-1)$ levels and $(2^{(\mathrm{M}+1)}-2)$ comparison thresholds. As an example, a 1b stage in a pipeline, algorithmic, or SAR ADC can be transformed to a 1.5b stage by replacing the comparator at $\{0\}$ with comparator at $\{-\mathrm{V_{FS}}/4$ and $\mathrm{V_{FS}}/4\}$, assuming a stage full-scale range of $\pm\mathrm{V_{FS}}$ as shown for a pipeline in Fig. 1(b). The input/output plot of the residue of a 1.5b pipeline ADC stage is shown in Fig. 1(c).

B. CRZ Redundancy

In half-bit redundancy, the additional comparison thresholds always surround the location of the integer (or conventional restoring) ADC levels, resulting in $(2^{(\mathrm{M}+1)}-2)$ comparison thresholds. In conventional restoring redundancy with Z added levels (CRZ), fewer levels are used than in the half-bit redundant case, but more than in the integer ADC [20], [21]. This, like half-bit redundancy, will allow for correction of over-range errors due to sub-ADC offsets and settling errors, but will have a smaller redundancy magnitude than half-bit redundancy. Also, in half-bit redundancy, the digital codes going to the sub-DAC are either integers or half-integers, resulting in low complexity digital recombination of stage digital outputs. However, digital outputs of a CRZ stage are more arbitrary, requiring additional digital processing at the conversion rate. Thus, there is a clear tradeoff with the CRZ scheme between the number of comparators and the loss in redundancy with greater digital complexity. One note is that [21] does achieve reduced digital complexity over [20] by changing the interstage gain of a pipeline stage, making the CRZ error correction logic look much more like that of a half-bit ADC. Example low-resolution full bit, half bit, and CRZ redundant stages are displayed in Fig. 2.

C. Sub-radix Redundancy

Sub-radix redundancy predates multilevel [5], [22] and is created not by adding comparison thresholds to a given stage, but rather by reducing the nominal ratio of a given stage full-scale range to that of the previous. As an example, a 1b per stage ADC would typically see the input referred full-scale range of each stage decrease by a factor of 2 with each cycle, effectively range scaling by $2^{(-\mathrm{ST})}$ where ST is the current stage and 2 is the given radix. In a sub-radix ADC, this radix of 2 would be replaced by something smaller like 1.7. A 1.7 radix makes the full-scale range of every stage slightly larger than the ideal full-scale range of the residue from the previous stage as demonstrated in Fig. 3. This allows over-range errors due to settling or sub-ADC nonlinearity to be captured and reshifted into the valid residue region of future stages.

Choosing the appropriate radix in sub-radix stages is often based on the tradeoff between the error tolerance that comes with a smaller radix and the reduced cycle count of a larger radix. It is also important to note that while this method can allow for a fixed single comparison device (important in SAR ADCs), it has the drawback of increasing DAC complexity due to the nonbinary nature of the stage subtraction [4] and/or a large digital engine [3], [23]. Almost always, this method is used in conjunction with DAC calibration.

D. Extra Stage Redundancy

Adding an extra cycle in a multistage ADC with a full-scale range that mirrors the full-scale range of the previous stage is a

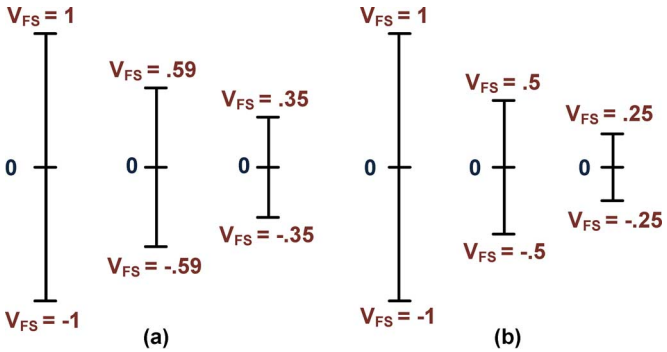

Fig. 3. 1b SAR stage full-scale ranges for: (a) sub-radix of 1.7 and (b) nonredundant binary stages.

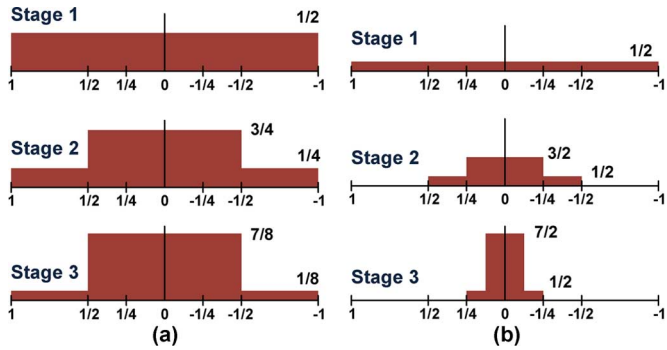

Fig. 4. Probability distribution function of the residue output of the first three stages for 1.5b/stage redundancy in: (a) pipeline ADC and (b) SAR ADC.

common redundancy method that allows for over-range errors to be shifted back into the ideal residue region. For a 1b/stage ADC, at the redundant stage, residue larger than the 0 comparator is subtracted by the V_{FS} of the stage and the residue smaller than 0 has V_{FS} added to it. This effectively swaps the ideal residue output of a stage across the 0 threshold level. Due to this swapping, any over-range error from $\pm V_{FS}$ to $\pm 2V_{FS}$ is now brought into the appropriate residue range ensuring that the final quantization error is now within $V_{LSB}/2$ of the current stage.

In its simplest form, extra stage redundancy can be implemented by replicating one or more stages in a multistage ADC and appropriately adjusting the digital summation block [24], [25]. Recently, more advanced techniques for SAR ADCs have been explored that preshift the input signal to allow for digital recombination that looks much like half-bit redundancy [26].

The following sections of this paper will demonstrate that multilevel redundancy not only compensates for over-range errors but also changes the statistics of the residue in each stage such that achieving extra resolution is possible. CRZ, sub-radix and extra cycle redundancy also affects stage residue statistics, but unlike multilevel, they either do not result in inherently improved resolution or give only partial shaping.

III. Ideal Residue Shaping

Half-bit redundant multistage ADCs have the ability to shape the PDF of the residue at the output of every distinct stage. This will be shown and analyzed first with a basic 1.5b/stage pipeline and will be extended to higher order half-bit redundancies. For a full pipeline to be designed with PDF residue shaping effects, architectural modifications should be made to the back-end ADC and will be described.

A. Residue Shaping in a 1.5b/stage Pipeline ADC

For a generic 1.5b/stage pipeline ADC, let us assume that the input signal probability is uniformly distributed for simplicity, and comparator thresholds are at their optimal locations of $\pm V_{FS}/4$ in each stage. The pipeline ADC multiplying digital to analog converter (MDAC) will quantize, subtract, and amplify the previous stage residue resulting in the following stage transfer function:

$$V_{OUT,STAGE} = \begin{cases} 2\left(V_{IN} - \frac{V_{FS}}{2}\right) & \text{for} \quad V_{IN} > \frac{V_{FS}}{4} \\ 2V_{IN} & \text{for} \quad \frac{-V_{FS}}{4} < V_{IN} < \frac{V_{FS}}{4} \\ 2\left(V_{IN} + \frac{V_{FS}}{2}\right) & \text{for} \quad V_{IN} < \frac{-V_{FS}}{4} \end{cases} \tag{1}$$

where the full-scale range of the sub-ADC is $\pm V_{FS}$.

After each stage, the residue of the codes that were within $\pm V_{FS}/4$ will remain in the center half of the next stage full-scale range since there was no subtraction performed. Codes above and below this central region experience a subtraction of $\pm V_{FS}/2$ which shifts them towards the center of the next stage full-scale range. The result is that after each stage, the PDF of the residue becomes more concentrated in the center half of the stage full-scale range. This phenomena is what we call PDF residue shaping and is illustrated in Fig. 4. It is important to note that a 1b/stage pipeline with an uniform input distribution will ideally maintain that distribution at the input of each stage. The expansion of (1) can then be used to derive the magnitude of the residue PDF change per stage

$$\Delta H_{PDF,STAGE} = \begin{cases} -\frac{H_{PDF,ST-1}}{2} & \text{for} \quad V_{IN} > \frac{V_{FS}}{4} \\ \frac{1-H_{PDF,ST-1}}{2} & \text{for} \quad \frac{-V_{FS}}{4} < V_{IN} < \frac{V_{FS}}{4} \\ -\frac{H_{PDF,ST-1}}{2} & \text{for} \quad V_{IN} < -\frac{V_{FS}}{4} \end{cases} \tag{2}$$

where ST is the stage being analyzed and H is the magnitude of the PDF.

The resulting integrated PDF of the residue after each MDAC stage can then be given by

$$\text{PDF(Stage)} = \begin{cases} \frac{1}{2^{ST+1}} & \text{for} \quad V > \frac{V_{FS}}{2} \\ 1 - \frac{1}{2^{ST}} & \text{for} \quad \frac{-V_{FS}}{2} < V < \frac{V_{FS}}{2} \\ \frac{1}{2^{ST+1}} & \text{for} \quad V < \frac{-V_{FS}}{2} \end{cases} \tag{3}$$

From Fig. 4 and (3), one can see that with the PDF residue shaping trend continuing for many stages, the residue in the final stage of a pipeline ADC will be squeezed into nearly 1/2 the full-scale range of that stage as shown in Fig. 5. By discarding the codes outside the center region, almost 6dB of extra resolution can be gained due to the minimization of the quantization error. A similar result was briefly mentioned in [27] in the context of pipeline residual distribution propagation analysis. The exact resolution increase can be determined by calculating the final number of codes shifted into center half of the full-scale range and number of total pipeline stages.

From (3), assuming the total number of bits in the pipeline should ideally equal the number of 1.5b stages plus 1, then the total number of levels in the center half of the last MDAC output is given by the following:

$$\begin{aligned} \text{Nlev} &= \left(1 - \frac{1}{2^{ST}}\right) 2^{ST+1} \\ &= 2^{ST+1} - 2. \end{aligned} \tag{4}$$

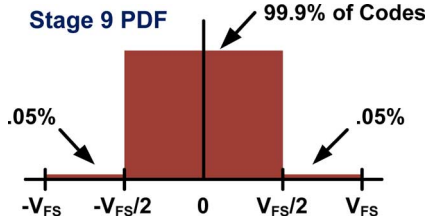

Fig. 5. Probability distribution function of the residue output of the 9th stage in a pipeline ADC.

This equation shows that there are always two effective levels missing from the center half of the final MDAC output. By tracing the shaping pattern of (1) across many stages, these two discarded levels are shown to be the top and bottom levels in the initial input and discarding them is synonymous to reducing the dynamic range of the pipeline input. This also means that PDF residue shaping occurs irregardless of the input distribution, such as sine or gaussian. The impact on the signal to quantization noise ratio (SQNR) of the ADC from this discarding can be calculated by first defining SQNR based on the number of quantization levels in an ADC. From [28], for a uniform quantization error

$$\begin{aligned}\mathrm{SQNR} &= 20\log_{10}\left(\frac{\mathrm{V_{FS}}}{2\sqrt{2}}\cdot\frac{\sqrt{12}(\mathrm{NLev})}{\mathrm{V_{FS}}}\right)\\ &= 20\log_{10}(\mathrm{NLev})+1.76. \end{aligned}\tag{5}$$

By inserting (4) into (5), the total SQNR due to ideal residue shaping is given as

$$\mathrm{SQNR_{ResidueShaped}} = 20\log_{10}(2^{\mathrm{ST}+1}-2)+1.76. \tag{6}$$

The improvement over a typical pipeline configuration where residue shaping is not considered is then given by

$$\begin{aligned}\Delta\mathrm{SQNR_{R-Shaped}} &= \mathrm{SQNR_{R-Shaped}}-\mathrm{SQNR_{Traditional}}\\ &= 20\log_{10}(2^{\mathrm{ST}+1}-2)-20\log_{10}(2^{\mathrm{ST}})\\ &= 20\log_{10}\left[2(1-2^{-\mathrm{ST}})\right]. \end{aligned}\tag{7}$$

From (7) one can see that given a reasonable number of pipeline 1.5b pipeline stages, the change in resolution is very close to 6 dB and can be treated as an extra bit of resolution in most quantization noise limited applications. This same analysis and resolution result is also directly applicable to SAR ADCs with 1.5b/stage redundancy.

B. Higher Order Half-Bit Redundant PDF Residue Shaping

Half-bit redundancy structures higher than 1.5b/stage will also shape the input residue across the stages of the pipeline resulting in an extra bit of resolution. For a 2.5b/stage pipeline, the MDAC transfer function of (1) can be modified as follows:

$$\mathrm{V_{OUT,STAGE}} = \begin{cases} 4\left(\mathrm{V_{IN}}-\frac{3\mathrm{V_{FS}}}{4}\right) & \text{for} \quad \mathrm{V_{IN}} > \frac{5\mathrm{V_{FS}}}{8} \\ 4\left(\mathrm{V_{IN}}-\frac{2\mathrm{V_{FS}}}{4}\right) & \text{for} \quad \frac{3\mathrm{V_{FS}}}{8} < \mathrm{V_{IN}} < \frac{5\mathrm{V_{FS}}}{8} \\ 4\left(\mathrm{V_{IN}}-\frac{\mathrm{V_{FS}}}{4}\right) & \text{for} \quad \frac{\mathrm{V_{FS}}}{8} < \mathrm{V_{IN}} < \frac{3\mathrm{V_{FS}}}{8} \\ 4\mathrm{V_{IN}} & \text{for} \quad \frac{-\mathrm{V_{FS}}}{8} < \mathrm{V_{IN}} < \frac{\mathrm{V_{FS}}}{8} \\ 4\left(\mathrm{V_{IN}}+\frac{\mathrm{V_{FS}}}{4}\right) & \text{for} \quad \frac{-3\mathrm{V_{FS}}}{8} < \mathrm{V_{IN}} < \frac{-\mathrm{V_{FS}}}{8} \\ 4\left(\mathrm{V_{IN}}+\frac{2\mathrm{V_{FS}}}{4}\right) & \text{for} \quad \frac{-5\mathrm{V_{FS}}}{8} < \mathrm{V_{IN}} < \frac{-3\mathrm{V_{FS}}}{8} \\ 4\left(\mathrm{V_{IN}}+\frac{3\mathrm{V_{FS}}}{4}\right) & \text{for} \quad \mathrm{V_{IN}} < \frac{-5\mathrm{V_{FS}}}{8} \end{cases}\tag{8}$$

This results in an integrated residue PDF after each MDAC stage of

$$\mathrm{PDF(Stage)} = \begin{cases} \frac{1}{2^{2(\mathrm{ST})+1}} & \text{for} \quad \mathrm{V} > \frac{\mathrm{V_{FS}}}{2} \\ 1-\frac{1}{2^{2(\mathrm{ST})}} & \text{for} \quad \frac{-\mathrm{V_{FS}}}{2} < \mathrm{V} < \frac{\mathrm{V_{FS}}}{2} \\ \frac{1}{2^{2(\mathrm{ST})+1}} & \text{for} \quad \mathrm{V} < \frac{-\mathrm{V_{FS}}}{2} \end{cases}\tag{9}$$

Generalizing this result to all multilevel stages we get

$$\mathrm{PDF(Stage)} = \begin{cases} \frac{1}{2^{\mathrm{M(ST)}+1}} & \text{for} \quad \mathrm{V} > \frac{\mathrm{V_{FS}}}{2} \\ 1-\frac{1}{2^{M(\mathrm{ST})}} & \text{for} \quad \frac{-\mathrm{V_{FS}}}{2} < \mathrm{V} < \frac{\mathrm{V_{FS}}}{2} \\ \frac{1}{2^{\mathrm{M(ST)}+1}} & \text{for} \quad \mathrm{V} < \frac{-\mathrm{V_{FS}}}{2} \end{cases}\tag{10}$$

where M is the number of full bits resolved from a given sub-ADC stage (i.e. M = 2 for a 2.5b stage).

From (10) the number of levels within the center half of the final MDAC stage can then be shown to be

$$\begin{aligned}\mathrm{Nlev} &= \left(1-\frac{1}{2^{\mathrm{M(ST)}}}\right)2^{\mathrm{M(ST)}+1}\\ &= 2^{\mathrm{M(ST)}+1}-2. \end{aligned}\tag{11}$$

This shows that for an M.5b/stage ADC, residue shaping will still allow for all but 2 of the levels to be shaped into the center half of the final MDAC stage. By following the derivation of (5)–(7), the total generalized half-bit SQNR improvement is given by

$$\Delta\mathrm{SQNR_{R-Shaped}} = 20\log_{10}\left[2\left(1-2^{-\mathrm{M(ST)}}\right)\right]. \tag{12}$$

Thus, while the higher number of comparison levels per stage presents a tradeoff between sub-ADC power and the number of overall pipeline stages, it does not affect the resolution improvements due to PDF residue shaping.

C. Ideal Back-end ADC Design

Typically, the final stage of a multistage ADC is a basic flash converter since there is no further subtraction or residue amplification after the final quantization stage. While exotic back-end ADCs exist [29], Fig. 6 shows some traditional 2b back-end flash stages that would be suitable for a pipeline or algorithmic structure. Since residue shaping has reduced the effective quantization error by a factor of 2, these 2b back end stages will only provide 1 bit of extra resolution. As an example, a 9-stage pipeline with a 2b traditional back-end flash ADC can have 11 total bits of resolution. However, by reducing the comparator threshold levels and back-end digital gain (radix value) by a factor of 2 (Fig. 6(c)), the full-scale range of the back-end flash matches that of the output reside and a full 2 bits of resolution can be gained. Thus, a 9-stage pipeline ADC with scaled 2b back-end can achieve 12 total bits of resolution.

The choice of optimal backend stage thresholds is illustrated in Fig. 7. Here the symmetrical threshold levels are swept from 0 to $\pm\mathrm{V_{FS}}$ with digital gains of 1 (traditional) and 1/2. One can see that due to PDF residue shaping, the 2b back-end ADC achieves an optimal resolution with comparison thresholds at $\pm\mathrm{V_{FS}}/4$ and a back-end gain of 1/2×. Also, the achievable resolution flattens when the output comparison levels extend beyond $\pm\mathrm{V_{FS}}/2$ since the residue is only located in the center half of the full scale range and thresholds beyond this region do

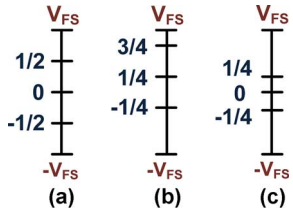

Fig. 6. 2b back-end flash stages for a: (a) traditional symmetrical back-end stage; (b) shifted back-end stage; and (c) compressed symmetrical back-end.

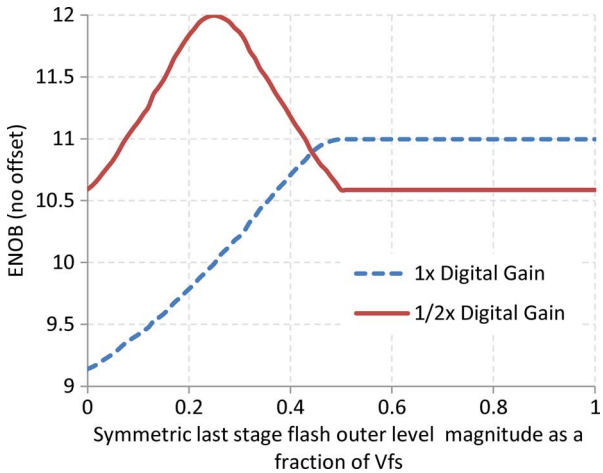

Fig. 7. 9×1.5 b/stage pipeline ADC with 2b back-end stage symmetric outer levels swept from 0 to $\pm V_{FS}$ and digital gains of 1 and 1/2.

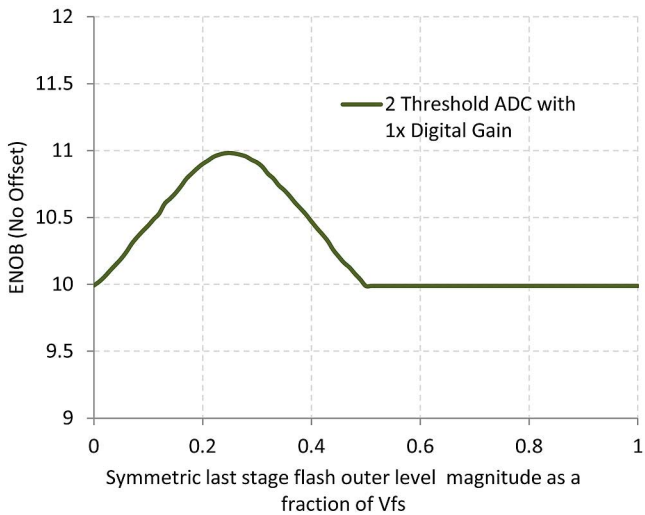

Fig. 8. 9×1.5 b/stage pipeline ADC with 3-level (2 threshold) back-end stage symmetric levels swept from 0 to $\pm V_{FS}$ and digital gain of 1.

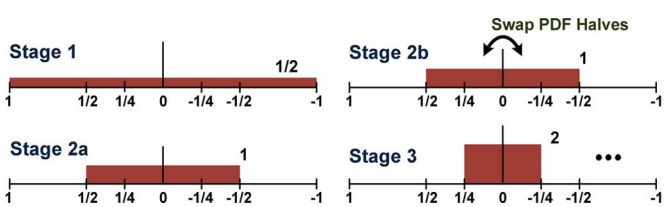

Fig. 9. Extra cycle redundancy stage PDF shaping diagram for a SAR ADC showing no PDF residue shaping in the redundant stage.

not provide any accuracy benefit. Finally, Fig. 7 illustrates that scaling the comparison thresholds to $\pm V_{FS}/4$ but not scaling the digital gain will result in a loss of 6 dB due to the misalignment of the back-end ADC levels and corresponding digital codes.

It should be noted that using this scaled back-end in a pipeline ADC will also reduce the number of unique reference levels that must be generated since $\{-V_{FS}/4, 0, V_{FS}/4\}$ are all used in either the sub-ADCs or MDAC subtraction. Furthermore, the number of bits in the back-end ADC will not affect the overall resolution improvement from PDF residue shaping since (4) will turn into

$$\text{Nlev} = (2^{\text{ST}+1} - 2)2^{\text{F}} \tag{13}$$

where F is the number of flash ADC bits. This equation yields the same SQNR improvement as (12) including the impact of the 2 lost levels in (11).

D. Shifted Back-end ADCs

Traditionally, the ADC of Fig. 6(a) has been used as a back-end 2b flash stage for a 1.5b/stage pipeline ADC, and it has been shown that Fig. 6(c) would be a more optimal choice. However the back-end of Fig. 6(b) has also been popular in literature [7], [30] due to the use of similar reference levels to the other sub-ADC stages and the assumption that if codes are shifted, then 3 levels are needed in the last stage to absorb the shifted residue range. This ADC is used to achieve the traditional 2b of extra resolution, however if one falsely assumes that the residue in the last stage is uniformly distributed between $\pm V_{FS}$, then this 2b of resolution is clearly not achievable due to the large quantization error on one end of the residue curve. The actual reason this back-end stage give 2 bits is also not due to a shifting of the last stage residue, but is because of the residue shaping effects previously described. Because of PDF residue shaping, the full-scale range of the residue is captured between the bottom two reference levels $(\pm V_{FS}/4)$ of Fig. 6(b), and this gives two bits due to the digital coding. The top comparison level $(3V_{FS})$ ideally does not affect the resolution with the exception of adding one extra code to the full-scale range. This is demonstrated in Fig. 8 where only 2 thresholds (3 levels) are swept from 0 to $\pm V_{FS}$ with digital output codes of 00, 01, and 10 at a gain of 1. The plot shows that even with the top level removed, two levels equally spaced at $\pm V_{FS}/4$, with nominal digital code gain, will produce 2 bits similar to the back-end ADCs of Fig. 6(a) and 6(b).

E. Extra Cycle, Sub-Radix, and CRZ Stage Shaping

While multilevel techniques are not the only way to implement redundancy to prevent settling and sub-ADC nonlinearity errors, it is the only variety that residue shapes to give a full bit of extra resolution. This is due to the fact that some residue is held without subtraction for the following stage, resulting in a residue transfer curve that grows in the center in each successive stage.

In extra cycle redundancy, an integer bit per stage operation is performed for numerous cycles followed by a redundant stage that mirrors the previous in terms of subtraction and/or interstage gain. Fig. 9 illustrates that because of the integer stage quantization, no stage residue shaping occurs. Furthermore, in the redundant cycle, the positive and negative PDF regions simply swap locations across the center comparison

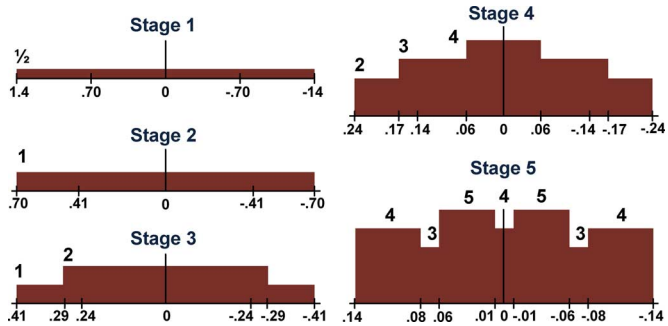

Fig. 10. Sub-radix redundancy stage PDF shaping diagram showing no PDF residue shaping for a SAR ADC with radix of 1.7.

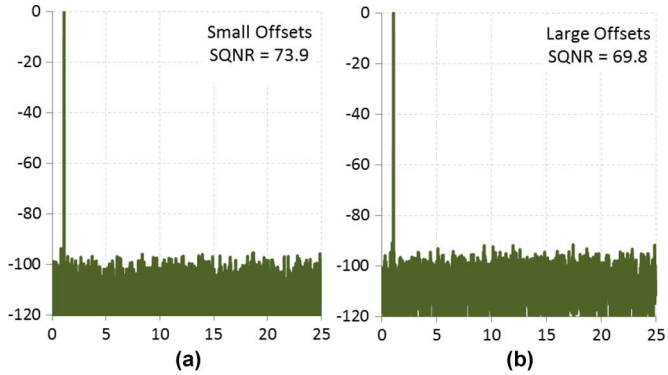

Fig. 11. FFT plots of a 12b quantization limited, PDF residue shaped 1.5b/stage pipeline ADC with normally distributed sub-ADC offsets of: (a) $0.024^{*}\mathrm{V_{FS}}$ and (b) $0.24^{*}\mathrm{V_{FS}}$.

threshold. While allowing for the correction of over-range signals, this swapping behavior does not result in increased inherent resolution. Additionally, even though the summation technique of [26] looks similar to that of half-bit redundancy, the single bit per cycle operation is still used, thus does not allow for shaping to occur.

In sub-radix redundancy, an integer bit per stage operation is again performed, but with the full-scale range of each successive stage being larger than the full-scale range of the residue in the previous stage. Fig. 10 demonstrates that while this initially makes the residue look like it is being shaped, the integer quantization per stage makes codes near a comparison threshold always be pushed to the outside of the permissible residue range after a few stages, where this number of stages is related to the chosen radix. While sub-radix redundancy will cause unusual interstage PDF residue transfer curves, it also does not provide the opportunity for additional resolution.

CRZ redundancy will shape the residue across many stages. However, the ideal output residue range of each stage is more than $\pm\mathrm{V_{FS}}/2$ because the spacing of the fewer comparison thresholds are larger. This means that the final shaped output will be between half the full-scale range and the full-scale range. This will result in a small amount of resolution improvement if the correctly scaled back-end ADC is chosen and digital codes are scaled, but not a full bit. Redesigning a given CRZ redundant ADC for full residue shaping will be described later.

IV. Residue Shaping Response to Non-Idealities

Reside shaping has been shown to give a 6 dB resolution improvement for multistage ADCs with multilevel redundancy when the comparison position is set at the optimal threshold. However, physically, perfect thresholds are not possible due to inherent offsets resulting from device sizing and power consumption limits [31]. Furthermore, the variability of sub-ADC comparison levels and settling nonidealities is the main reason for using redundancy in the first place.

A. Analysis of Offsets in Residue Shaping

Offsets or settling errors in multilevel redundant ADC stages will affect the residue shaping differently in each stage and under specific conditions. These effects can be understood by analyzing the result of a sub-ADC threshold offset on the overall PDF residue shaping in a 1.5b/stage SAR ADC. A SAR is chosen as an example due to the simplicity of examining subtraction across many stages. With an offset, the residue operation of (1) changes to

$$\mathrm{V_{OUT,STAGE}} = \begin{cases} \left(\mathrm{V_{IN}} - \frac{\mathrm{V_{FS}}}{2}\right) & \text{for} \quad \mathrm{V_{IN}} > \frac{\mathrm{V_{FS}}}{4} + \Delta \\ \mathrm{V_{IN}} & \text{for} \quad \frac{-\mathrm{V_{FS}}}{4} < \mathrm{V_{IN}} < \frac{\mathrm{V_{FS}}}{4} + \Delta \\ \left(\mathrm{V_{IN}} + \frac{\mathrm{V_{FS}}}{2}\right) & \text{for} \quad \mathrm{V_{IN}} < \frac{-\mathrm{V_{FS}}}{4} \end{cases} \tag{14}$$

where in the SAR case, $\mathrm{V_{FS}}$ corresponds to a given stage full-scale range, which in a binary weighted SAR will decrease by a factor of two in each cycle.

A stage with comparator offsets will move some residue close to the ideal $\pm\mathrm{V_{FS}}/4$ thresholds to outside the center half of the next stage full-scale range ($\pm\mathrm{V_{FS}}/2$ of $[\mathrm{stage}+1]$) before being quantized by that next stage. If this offset is small, the next SAR stages will reshift the error back into the center half of the following full-scale ranges. However if the offset is so large that it cannot be shifted back into the center half of the final full-scale range ($\pm\mathrm{V_{FS}}/2$ of the final stage), then the PDF of the final stage output will show quantization leakage beyond $\pm\mathrm{V_{FS}}/2$, degrading the resolution improvement.

In the cases where quantization leakage occurs due to large random comparator offsets, the error does not cause distortion but rather raises the SQNR noise floor since the error mostly is uncorrelated with the input and the stage input becomes increasingly white with each progressing stage [27]. This is graphically shown in Fig. 11 where the FFT of a 12b quantization limited, PDF residue shaped ADC noise floor rises with increasing comparator offset. Additionally, since excessive comparator offset creates a slightly larger than normal code bin followed by a slightly smaller one, this comparator offset will show up as periodic DNL as plotted in Fig. 12. The DNL periodicity and the fact that this offset will occur mostly for latter stages, means that the INL does not show any global curvature.

Since redundancy helps to fix small comparator offsets before they cause quantization leakage, it is possible to derive bounds for the comparator offset in each stage showing the tolerable offset that will cause no SQNR degradation. The allowable comparator offset for optimal residue shaping is equal to the maximum subtraction available from the stages following the offset stage that can bring an offset code that is outside the current stage redundant center half, back into the center half of the last stage full-scale range. Continuing with the 1.5b/stage SAR, the

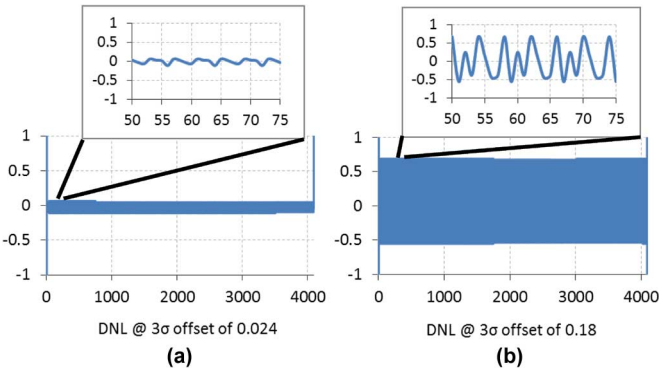

Fig. 12. DNL plots of a 12b PDF residue shaped pipeline ADC showing periodic DNL curves for a normal distributed offset of: (a) $0.024^{*}\mathrm{V_{FS}}$ and (b) $0.18^{*}\mathrm{V_{FS}}$.

total DAC subtraction from a given stage that is available, assuming a normalized input full-scale range of 1, is

$$\begin{aligned}\mathrm{DACSubtraction_{Total}} &= \sum_{\mathrm{k=ST-1}}^{\mathrm{N-1}} \left(\frac{1}{2^{\mathrm{k}}}\right) \\ &= \frac{1}{2^{\mathrm{ST}}} - \frac{1}{2^{\mathrm{N-1}}} \end{aligned} \tag{15}$$

where N is the total SAR resolution in bits including residue shaping with no back-end flash.

Any codes outside of the region where the following stage subtraction cannot pull that code into $\pm\mathrm{V_{FS}}/2$ of the last stage residue output, will then cause quantization leakage. This results in the following tolerable offset regions for error-free residue shaping in the 1.5b/stage SAR with an input full-scale range of ± 1

$$\mathrm{R\ Bounds_{SAR}} = \begin{cases} \text{Upper Bound} = \frac{1}{2^{\mathrm{ST}}} - \frac{1}{2^{\mathrm{N}}} \\ \text{Lower Bound} = \frac{1}{2^{\mathrm{N}}} \end{cases}. \tag{16}$$

It is important to note that the ideal comparator threshold is 1/4 of the full-scale stage voltage or $(1/2^{\mathrm{ST+1}})$. The bounds in the above equation do not represent offset deviations (as zero offset from the ideal threshold would be perfect) but rather the minimum and maximum absolute threshold locations to prevent resolution degradation.

Conceptually, the result of (16) can be understood by noting that the full-scale range of a SAR stage is in this case $(1/2^{\mathrm{ST+1}})$. Thus $(1/2^{\mathrm{ST}}) - (1/2^{\mathrm{N-1}})$ is the maximum amount of subtraction available if the current stage code is in the redundant zone. However, since the final full-scale residue range after the last SAR stage is $(1/2^{\mathrm{N-1}})$ and the final residue should be bounded between $\pm(1/2^{\mathrm{N}})$ for residue shaping, a code exactly at the stage comparison threshold of $(1/2^{\mathrm{ST}})$ will not fall into the bounded region due to the max allowable subtraction. Thus the maximum redundancy is bounded to $(1/2^{\mathrm{ST}}) - (1/2^{\mathrm{N}})$ and $(1/2^{\mathrm{N}})$ as opposed to the traditional boundings of $(1/2^{\mathrm{ST}})$ and 0 to prevent residue shaped quantization leakage errors. Note that in the SAR ADC, the last stage bounds show that comparator offsets in the final stages will slightly degrade the overall 6 dB resolution improvement from residue shaping, but will not cause the loss of overall net SQNR improvement.

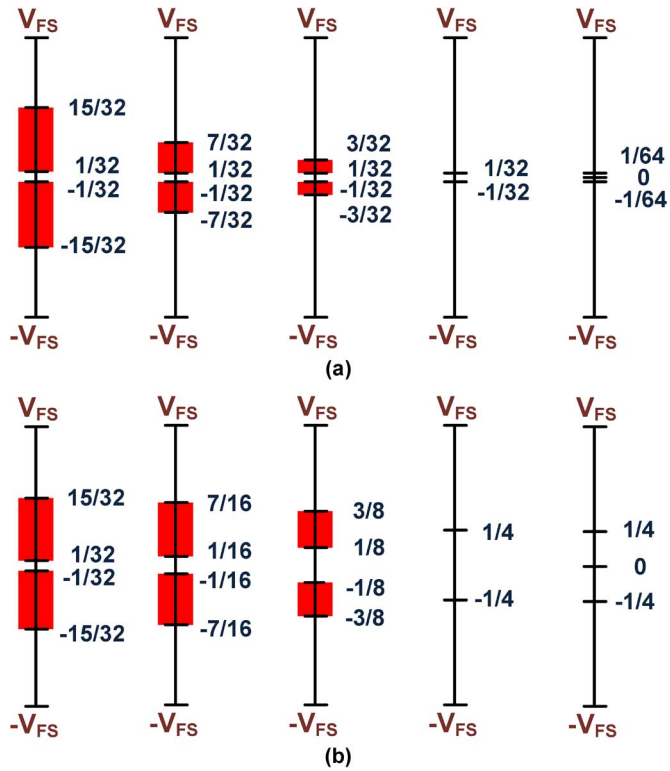

Fig. 13. Threshold offset range to maintain ideal residue shaping in: (a) a 4 × 1.5b/stage SAR ADC and (b) a 4 × 1.5b/stage Pipeline or Algorithmic ADC.

The result of (16) is again similar in the 1.5b/stage pipeline or algorithmic ADC with the addition of interstage gain

$$\mathrm{R\ Bounds_{Pipe}} \begin{cases} \text{Upper Bound} = \frac{\mathrm{V_{FS}}}{2} - \frac{\mathrm{V_{FS}}}{2^{\mathrm{N-ST+1}}} \\ \text{Lower Bound} = \frac{\mathrm{V_{FS}}}{2^{\mathrm{N-ST+1}}} \end{cases} \tag{17}$$

where N is again the total pipeline resolution in bits including the bit from residue shaping.

This result is similar, but slightly more stringent than the traditional pipeline comparison threshold over-range criteria of $(\mathrm{V_{FS}}/2)$ and 0.

These pipeline and SAR 1.5b/stage results are shown graphically in Fig. 13. Similar analysis performed for higher order multilevel redundancy yields the following bounds for M.5 bit pipeline ADCs

$$\begin{aligned}&\mathrm{R\ Bounds_{Pipe\_Mulit-bit}} \\ &\quad = \begin{cases} \text{Upper Bound} = \frac{\mathrm{V_{FS}}}{2^{\mathrm{M}}} - \frac{\mathrm{V_{FS}}}{2^{\mathrm{N-M(ST)+1}}} \\ \text{Lower Bound} = \frac{\mathrm{V_{FS}}}{2^{\mathrm{N-M(ST)+1}}} \end{cases}. \end{aligned} \tag{18}$$

These bounds are defined as the maximum and minimum allowable spacings of the two M.5b redundant thresholds surrounding an M-bit sub-ADC comparison threshold for ideal residue shaping.

B. ADC Design for Optimized PDF Residue Shaping

Comparing the allowable offset range in a traditional structure to that of the residue shaped structure, one can see that the early and back-end stages are nearly identical in terms of allowable offset or redundancy magnitude. In the PDF residue shaped structure, only the last couple of stages before the back-end ADC have offset bound requirements that are noticeably stricter

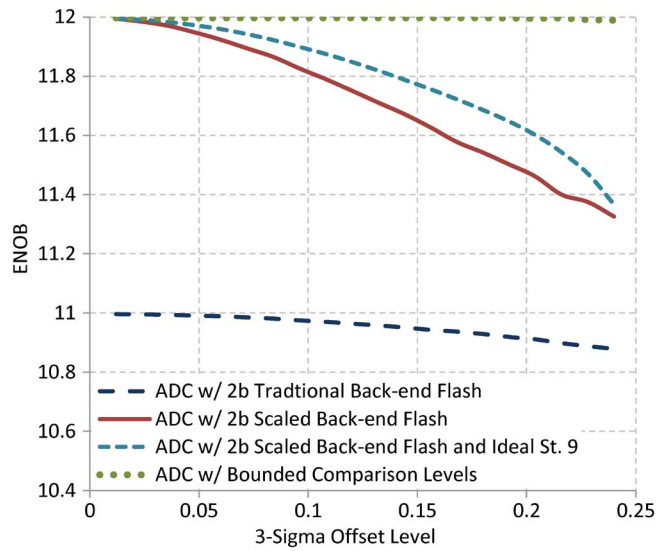

Fig. 14. 9-stage ADC resolution comparison with a traditional symmetric back-end, proposed scaled back-end, ideal back-end, and bounded comparison levels.

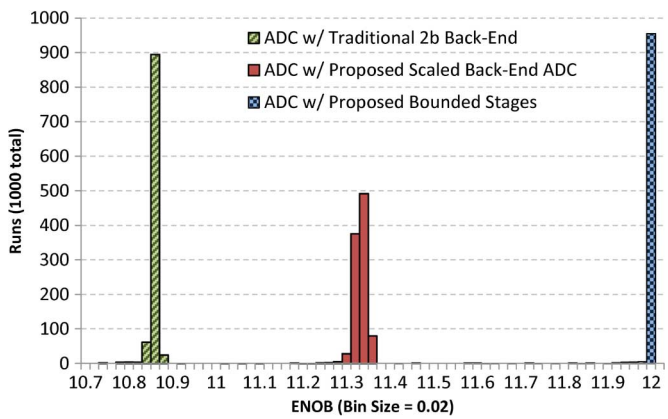

Fig. 15. Histogram showing the ENOB distribution of 1000 runs of 9-stage pipeline ADCs with a traditional symmetric back-end, a proposed scaled back-end and a bounded comparison level back-end, all at a 3-sigma offset level of 0.2.

than in the traditional ADC. However, this typically does not greatly degrade the 6 dB SQNR improvement since large redundancy is still available in the early stages for SAR settling error reduction and the SQNR degradation from to quantization leakage due to comparator thresholds exceeding offset bounds in pipeline ADCs is reduced in the latter stages due to the prior interstage gain. Also if slightly greater effort is placed on reducing the offsets in only the last couple stages of a multistage ADC, there can be large gains in offset tolerance.

Fig. 14 illustrates the 100 run average final resolution vs. normally distributed comparator offsets for a 9-stage pipeline ADC with 2b back-end flash for a sinusoidal input. The traditional 2b flash of Fig. 6(a) is compared with the proposed scaled 2b flash of Fig. 6(c). Since the scaled flash full scale range matches the actual full-scale range of the ideal quantization error, the extra bit of resolution described in (7) is achieved. The scaled version however does lose resolution, as the nominal comparator offset is increased, at a slightly faster rate than the traditional structure due to the large offsets exceeding the redundancy bounds placed on MDAC sub-ADC stages in (17) causing quantization leakage. However, even with this degradation, the resolution is still better for all offset conditions before the maximum 3-sigma offset of $\pm V_{FS}/4$ is reached and for a typical design where the 6-sigma offset is $0.25^{*}V_{FS}$ there is still greater than 4 dB of average resolution gain. Also shown in Fig. 14 is a 9-stage ADC with scaled back-end ADC that has an ideal 9th stage sub-ADC. By making the last shaping stage offsets smaller through slight comparator size increases, there can be significant resolution improvements in the presence of large variation over just scaling the back-end. Finally, a 9-stage pipeline with the bounded comparison offset threshold limits of (17) and Fig. 13 are shown. This results in a nearly ideal 1b of resolution improvement until over-range errors degrade the performance near offset levels of $V_{FS}/4$.

In order to understand the spread of the resolution at large comparator offsets, Fig. 15 shows a histogram of the 9-stage ADC ENOB values for the traditional symmetric, proposed symmetric, and proposed bounded back-end structures. Here we can see that for normally distributed offsets, the final ENOB spread of the PDF residue shaped ADC is only slightly larger than that of the traditional structure, which is important for ADC yield analysis.

When designing a multistage ADC it has been shown above that residue shaping can give extra resolution in a quantization noise limited system with very simple changes to the back-end ADC and digital error correction logic. In thermal noise limited designs, extra resolution may not be possible, however a pipeline stage or SAR cycle can be eliminated and the corresponding quantization made up from the PDF residue shaping property. In a pipeline this results in somewhat lowered power consumption, reduced area, reduced operational amplifier count, and lower latency. In the SAR ADC, residue shaping can eliminate an operation cycle saving both switching power, conversion delay, and comparison power. Also, the SAR DAC needs one less value in conventional binary-weighted capacitor arrays reducing cap spread and, in mismatch limited cases, reducing total cap area and power.

C. Modifications to CRZ ADCs for PDF Residue Shaping

CRZ ADCs will ideally reduce the maximum magnitude of the center residue after each stage. The ideal bound of the residue within the outer thresholds after each CRZ stage can be given by the following from [20]:

$$\mathrm{R\ Bound_{CRZ}} = \frac{2^{\mathrm{M}} - 1}{2^{\mathrm{M}} - 1 + \mathrm{Z}} \tag{19}$$

where Z is the number of additional threshold levels added from a typical M-bit stage.

It is clear that this architecture will only give partial residue shaping due to the increased threshold level sizes. However, from (17) it has been shown that only the final stage in a multistage pipeline needs to have the full and ideal half-bit redundancy to achieve 6 dB residue shaping. Thus the increased residue magnitude of the CRZ stages can be acceptable in earlier stages of the pipeline if the reduced comparator nonlinearity tolerance described in [20] is acceptable. Using the generalized redundancy bounds of (18) and the maximum residue for a

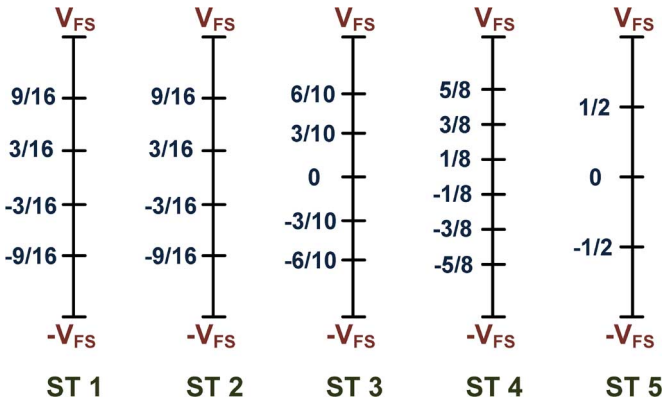

Fig. 16. Scaled 4-stage CRZ pipeline ADC with 2b backend flash for optimal residue shaping.

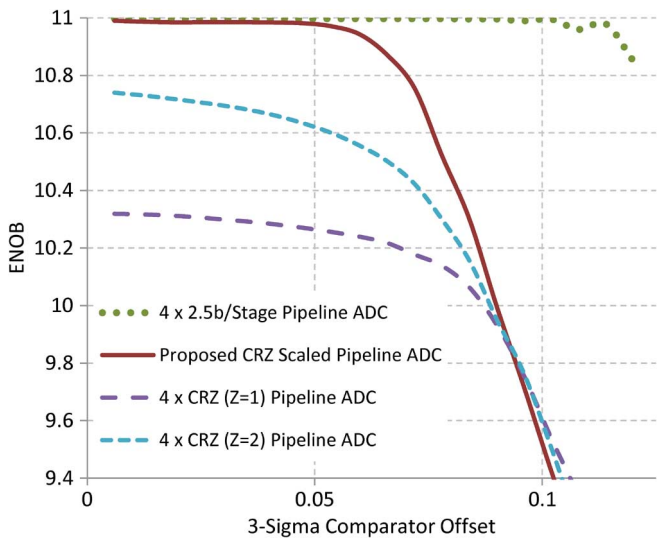

Fig. 17. Resolution vs. 3-sigma comparator offset for normal CRZ stages, scaled CRZ, and 2.5b/stage ADCs with ideal back-end and last stage comparison thresholds.

CRZ converter (19), the following shows conditions for full-bit residue shaping with a full-scale range of 1:

$$\begin{aligned} &\mathrm{R\ Bound_{CRZ}} < \mathrm{R\ Bound_{Pipe\_Multibit\_Output}} \\ &\frac{2^{\mathrm{M}}-1}{2^{\mathrm{M}}-1+\mathrm{Z}} < 2^{\mathrm{M}}\left(\frac{1}{2^{\mathrm{M}}}-\frac{1}{2^{\mathrm{N}-\mathrm{M(ST)}+1}}\right). \end{aligned} \tag{20}$$

The required Z additional levels for a given sub-ADC stage to achieve ideal residue shaping (assuming no comparator nonlinearity) is then given as

$$\begin{aligned} \mathrm{Z} &> \frac{2^{\mathrm{M}}-1}{2^{\mathrm{M}}\left(\frac{1}{2^{\mathrm{M}}}-\frac{1}{2^{\mathrm{N}-\mathrm{M(ST)}+1}}\right)} - 2^{\mathrm{M}}+1 \\ &> \frac{2^{\mathrm{M}}-1}{2^{-\mathrm{M(ST+1)}+\mathrm{N}+1}-1}. \end{aligned} \tag{21}$$

Fig. 16 shows an example 4 stage CRZ pipeline with 2b back-end sized from (20). The scaled pipeline consists of 2× 5-level CRZ stages followed by a 6-level CRZ stage for slightly increased stage redundancy, an ideal 2.5b stage and an ideal 2b backend flash. Fig. 17 shows the resulting scaled ENOB verses comparator offsets with a full $\mathrm{CRZ_{Z=1}}$, $\mathrm{CRZ_{Z=2}}$, and 2.5b/stage pipelines with ideal back-end and final pipeline stage comparison thresholds. By scaling the CRZ stages, the residue of each pipeline stage is ideally still within the PDF residue shaping range of the pipeline. However, since the number of early stage comparators have been reduced, the offset tolerance also reduces. Fig. 17 demonstrates these results by showing a pipeline of $\mathrm{CRZ_{Z=1}}$ and $\mathrm{CRZ_{Z=2}}$ stages which achieve less than 1b of added resolution due to PDF residue shaping. The scaled CRZ of Fig. 14 is also plotted in Fig. 17 which achieves the full 1b of resolution, but has a much lower offset tolerance when compared with the bounded pipeline structure of (18). Thus, scaled PDF residue shaped CRZ structures can make a lower power and complexity pipeline only if a smaller early stage redundancy range is not problematic, digital logic is cheap and reference generation is not expensive. Otherwise, half-bit redundant architectures with PDF residue shaping are typically the better choice.

Finally, it can be shown that the pipeline of [21] also uses non-half-bit multilevel redundant stages but can achieve full bit PDF residue shaping due to the manipulation of the interstage gain. The analysis follows that of (4)–(7) and has offset bounds similar to that of (18).

V. Conclusion

In this paper an analysis of PDF residue shaping was performed for multistage ADCs. PDF residue shaping results in nearly 6 dB of extra resolution for half-bit redundancy varieties due to the PDF of the residue being centered in the middle half of the final full-scale output range of the last ADC stage. This shaping was shown to not be present in extra-cycle and sub-radix redundancy with a partial presence in CRZ redundancy. An analysis of offset errors was also performed and a modified offset tolerant threshold region was derived. Finally, design suggestions were made to maximize the resolution of a given multistage ADC with residue shaping by identifying critical sub-ADC stages, describing the ideal back-end ADC gain, showing optimal 2b back-end ADC threshold levels, and describing optimized CRZ redundant ADCs.

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