A 10-b Ternary SAR ADC With Quantization Time Information Utilization

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***Abstract*—The design of a ternary successive approximation (TSAR) analog-to-digital converter (ADC) with quantization time information utilization is proposed. The TSAR examines the transient information of a typical dynamic SAR voltage comparator to provide accuracy, speed, and power benefits. Full half-bit redundancy is shown, allowing for residue shaping which provides an additional 6 dB of signal-to-quantization-noise ratio (SQNR). Synchronous quantizer speed enhancements allow for a shorter worst case conversion time. An increased monotonicity switching algorithm, stage skipping due to reference grouping, and SAR logic modifications minimize overall dynamic energy. The architecture has been shown to reduce capacitor array switching power consumption and digital-to-analog converter (DAC) driver power by about 60% in a mismatch limited SAR, reduce comparator activity by about 20%, and require only 8.03 average comparisons and 6.53 average DAC movements for a 10-b ADC output word. A prototype is fabricated in 0.13-μm CMOS employing on-chip statistical time reference calibration, supply variability from 0.8 to 1.2 V, and small input signal power scaling. The chip consumes 84 μW at 8 MHz with an effective number of bits of 9.3 for a figure of merit of 16.9 fJ/C-S for the 10-b prototype and 10.0 fJ/C-S for a 12-b enhanced prototype chip.**

***Index Terms*—Residue shaping, successive approximation analog-to-digital converter (SAR ADC), SAR ADC redundancy, SAR switching, ternary SAR (TSAR), time quantization.**

I. Introduction

In the evolving world of electronic circuits, improved analog-to-digital conversion performance is required in conjunction with high efficiency for today's mobile, sensor, and green applications. This is all taking place on the backdrop of ever-scaling process technologies optimized for digital CMOS density. One data-conversion architecture that has been shown to effectively combat scaling deficiencies for midresolution and speed requirements is the successive approximation (SAR) analog-to-digital converter (ADC). Currently, the SAR ADC can be found in a variety of applications from medical instrumentation to sensor nodes, body-area networks, and portable electronics.

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Due to the simple quantizer structure, lack of residue amplification, and high dependence on digital circuitry, the SAR ADC tends to be inherently energy-efficient. However, to meet the ever increasing energy and performance demands on the digitization of analog signals, a number of innovative developments have been recently proposed for the SAR ADC. The asynchronous SAR was demonstrated in [1] and can increase the effective overall speed of a SAR conversion by about a factor of two. However, the issue of missing bits due to midcycle metastability leads to either a larger bit error rate (BER) or increased critical path logic [2]. The variable window function SAR [3] reduces the required amount of switching to minimize the SAR input voltage, but requires extra voltage comparators and references with an accuracy that increases in each stage. SAR redundancy through subradix arrays [4], [5] and additional stages [6], [7] can reduce the settling time requirement of the capacitor bank, prevent early stage transient errors, and allow for the injection of calibration signals [8], [9], but at the expense of extra cycles and power consumption due to additional comparisons and digital complexity. Finally, a number of algorithms have been proposed to minimize switching power consumption in capacitive feedback DACs. These include subdividing the first DAC element-switching operations [10], switching in one element per phase [11], and switching differentially with the input signal sampled relative to the common mode [12], [13]. The final switching structure has been known as the merged capacitor switching (MCS) SAR and has been shown to maximally reduce switching energy when compared with other techniques.

In this paper, a new ternary SAR (TSAR) architecture is proposed that utilizes the MCS SAR quantizer transient information to provide enhanced speed, redundancy, and reduce power consumption. The paper is organized as follows. Section II will motivate and describe the TSAR structure, Section III will explore the inherent benefits of the structure, Section IV will show the architectural design choices that can optimize the performance and efficiency of the ADC, Section V will outline the proof of concept prototype implementation, Section VI will described the measured results, and conclusions will be given in Section VII.

II. SAR Quantizer Transient Response

A traditional binary capacitive SAR works by sampling the analog input signal and performing many cycles of 1-b comparisons, as illustrated in Fig. 1. After each 1-b decision, a DAC subtracts or adds a binary-weighted voltage to the quantizer input, minimizing the voltage difference and allowing the quantizer outputs to digitally represent the input signal through a binary search algorithm [14], [15]. A modern popular SAR

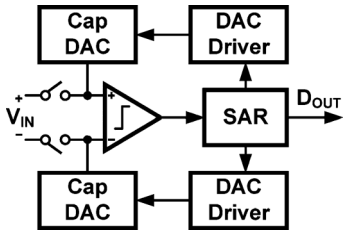

Fig. 1. Simplified top-plate sampled differential SAR ADC structure.

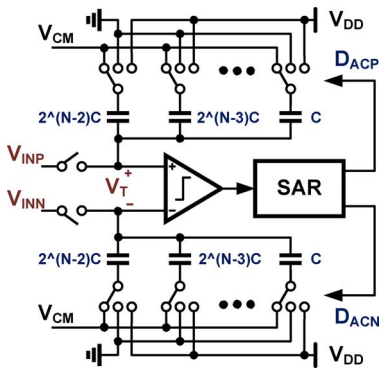

Fig. 2. Architecture of the MCS SAR structure [12] with a binary capacitive feedback DAC utilizing three reference levels.

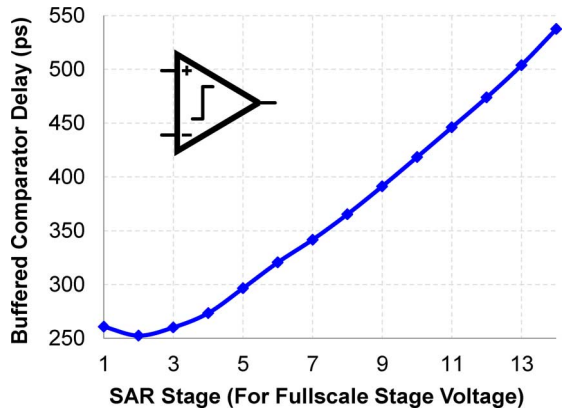

Fig. 3. Buffered comparator full-scale output delay *versus* SAR stage voltage, where the comparator input voltage equals the full-scale voltage of a given SAR stage.

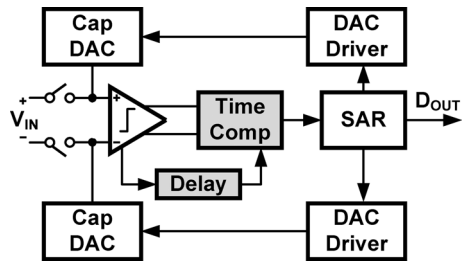

Fig. 4. Proposed TSAR block diagram with a time comparator and delay unit added.

architecture, the energy-efficient capacitive MCS structure, is shown in Fig. 2. Here, the input is sampled onto the top-plate virtual ground nodes of the capacitive DAC with respect to common-mode voltage V_{CM} in the sampling phase and these nodes float during the conversion. The conversion starts by strobing the 1-b voltage comparator which sends either a "1" or "0" quantized representation of the virtual ground inputs to the SAR logic. This logic will then trigger the bottom plate of the MSB capacitor in the DAC to switch to either VDD or GND in order to minimize the differential voltage on the virtual ground nodes. Thus, if the first comparator output is a "1," the bottom plate of the MSB capacitor on the top side of the SAR is switched to GND, and the bottom plate of the opposite MSB capacitor is switched to VDD. One can see from this switching operation that, in every phase, the bottom plate of each capacitor is switched from V_{CM} to either V_{DD} or G_{ND} starting with the MSB capacitor and progressing to the LSB with one capacitor per phase. Once the final digital word has been determined, the bottom plates of the whole capacitor DAC are reset to V_{CM}.

While this SAR operation performs with a low switching energy, one can see that there are a number of inefficiencies with the structure. The first is that, while there are three levels in the capacitive DAC, only two are being utilized as potential switchable states in each phase. The presence of three DAC levels in the capacitor array signifies that there are multiple switching trajectories that can be taken to reach a given virtual ground minimization, some of which may be more optimal than others. Furthermore, each phase must be sufficiently long to accommodate the worst case comparator delay since there is no redundancy present to correct sub-ADC errors. In order to fully utilize the MCS capacitive DAC and provide ancillary speed and accuracy benefits, one needs another source of information to dictate an optimized switching operation.

One such information source can be found by looking at the transient response of the voltage comparator. Assuming that the comparator has a typical single-pole response, the transfer function can be modeled as follows:

$$V_{\mathrm{OUT}} = (V_G) \exp\left[\frac{(A-1)\,t}{\tau}\right]. \tag{1}$$

where A is the comparator gain, V_G is the comparator input voltage, and τ is the time constant. While naturally exponential, this delay is shown to vary linearly with the full-scale voltage of each stage (which scales down by a factor of two per stage) in the SAR operation as follows:

$$t_{\mathrm{Stage}(N)} - t_{\mathrm{Stage}(N-1)} = \frac{\ln(2)}{\left[\frac{(A-1)}{\tau}\right]} = \frac{\ln(2)}{C}. \tag{2}$$

where C is simply a constant term. This variation is plotted in Fig. 3 from a transient simulation of a dynamic transistor-level comparator. Since the delay response is independent of the polarity of the virtual ground nodes, measuring the time delay of the comparator gives information about the absolute value of the input. Also, if the delay information were to be used to determine the magnitude of the input with respect to a percentage of a stage's full-scale range, the accuracy of that time measurement would not increase from one SAR stage to the next due to the linear comparator delay verses stage.

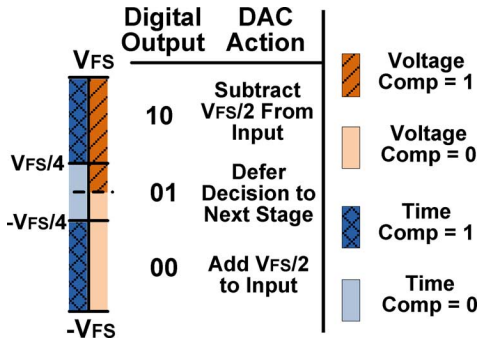

Fig. 5. Three-level TSAR stage digital output and DAC action based on voltage and time comparator outputs assuming $V_{FS}/4$ redundancy thresholds.

The proposed TSAR structure is shown in Fig. 4 [16]. Here, a time comparator and delay unit are introduced into the critical path of the SAR loop in a differential fashion. The purpose of the time quantizer structure is to determine if the input magnitude is smaller or larger than a given reference, with respect to the full-scale range of the given SAR stage, by examining the delay of the main voltage comparator. This time quantization is coarse and will feed to the SAR logic unit. The time quantization thresholds are set by a delayed voltage comparator clock. Other standalone time comparison structures have been proposed [17], [18], but this differs in that the time comparison does not set the SAR sub-ADC quantized output alone, but rather shifts the fine voltage comparator outputs to generate three levels per stage. This structure maintains the accuracy and global offset provided by the single traditional voltage comparator and enhances the MCS SAR operation, rather than attempting to just replace the voltage comparator with a time-based structure. Finally, a time comparator structure with voltage comparator was mentioned in [19], for the purpose of comparator metastability and last stage flash. However, that circuit does not take advantage of the power savings, accuracy improvements, and speed increases described in the remainder of this paper.

The operation of the TSAR core for a given sample begins with the master clock sampling the input onto the DAC virtual ground nodes and starting an internal core clock. This core clock generates a clock edge for the voltage comparator and delay unit. A delayed internal clock edge is then sent to the time quantizer. If the buffered output of the voltage comparator resolves to either a high or low code before the delayed clock latches the data on the time quantizers, then the output digital code for the stage is the standard "10" or "00." However, if the input does not flip the buffer inverters to either a high or low state before the delayed clock arrives to the time quantizer, the stage digital code sent to the SAR logic will be the mid code or "01" as illustrated in Fig. 5. The benefits of this ternary coding will be explored in the next sections.

III. TSAR Inherent Benefits

A. TSAR Redundancy

The TSAR structure has a number of inherent benefits due to the magnitude information generating a third level in each stage. The first is the presence of a redundancy that looks like the 1.5-b/stage type seen in pipelined converters [20], [21]. This redundancy is useful for tolerating small settling errors or preventing over-range errors from sampling transients. Also, as in a pipelined converter, sub-ADC reference levels can vary from $V_{FS}/2$ to 0 without causing over-range errors in later stages. This voltage-domain requirement becomes more relaxed in the time domain for the TSAR since there is a set time value that corresponds to the upper redundancy limiting $\pm V_{FS}/2$ level (where V_{FS} refers to the full-scale voltage of a given TSAR stage), but not the 0 level, which would require an infinite time delay. This implies that in chips with large dynamic supply and temperature variation, redundancy over-range problems can be mitigated by simply designing for a smaller initial redundancy range. Additionally, the fine comparator still decides the final polarity of a signal, so that the offset of that fine voltage comparator is still the global offset of the SAR. Finally, since the voltage comparator delay varies linearly with the TSAR stage scaling, as shown in Fig. 3, there is no increased time comparator accuracy requirements in later stages as would be the case if the redundancy were implemented in the voltage domain.

This time based redundancy has a great advantage over the other traditional SAR redundancy schemes of subradix [4], [5] or extra stage [6], [7] in that no additional cycles are needed and the capacitor DAC array can still be binary weighted for simplified matching and digital logic. Furthermore, the digital error correction addition of 1.5-b/stage pipelined structures [20] can still be employed here without any analog shifting.

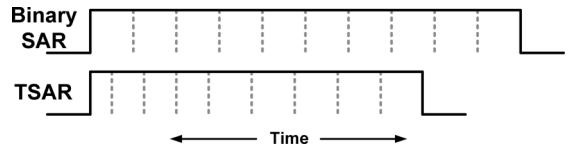

Fig. 6. Binary and TSAR synchronous conversion speed illustrative comparison with internal phases noted. Both the TSAR and binary SAR are synchronous and have a fixed conversion delay.

B. Speed Improvements and Activity Reduction

The TSAR time comparator also has built-in speed benefits. Like the asynchronous SAR, the TSAR does not wait for the worst case input-dependent delay of the voltage comparator to resolve the rest of the bits in the SAR conversion. Rather, after the delayed clock strobes the time comparators, the TSAR loop clocks the critical path logic and DAC whether or not the voltage comparator has resolved. This timing structure is still synchronous, however, since every cycle is deterministically ended with the delayed internal clock edge, even in the case of voltage comparator metastability. When compared with a traditional synchronous SAR, the TSAR structure allows for the largest time savings in early stages. In the traditional synchronous structure, the SAR must wait for the worst case delay from an input of $\pm V_{LSB}/2$ in each stage while the TSAR must only wait for an input larger than the redundancy region, often $\pm V_{FS}/4$, as illustrated in Fig. 6. In all, the worst case SAR conversion delay is significantly reduced.

The TSAR structure also increases the efficiency of the DAC switching and drivers by eliminating switching operations when the input is differentially small. When the input is within both time comparator thresholds, no switching operation is

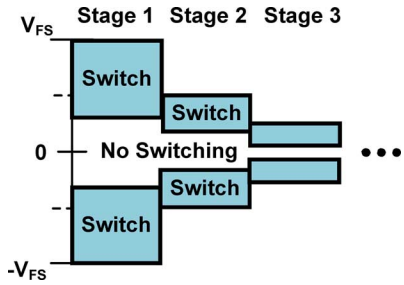

Fig. 7. DAC activity windowing effect though the implementation of a no-switching region for codes within the TSAR redundancy range for MSB stages.

performed, meaning that no capacitor switching power or DAC driver power is used in that phase as illustrated in Fig. 7. This power-saving switching method is similar to the windowed SAR of [3], however, there, voltage comparators were used to create the windowing function and here that operation is pushed to the time domain. In the voltage domain, the accuracy of the extra voltage comparators has to increase by a factor of two in each stage for effective power savings, thus their useful operation is only in the first few stages. The accuracy of the comparator in the time domain does not increase from one stage to the next though, due to the exponential nature of the comparator delay, allowing the windowing to be effectively applied to the whole SAR. While the energy savings of the DAC drivers and capacitor array windowing reduces by a factor of two in each stage, it will be shown that, by adjusting this window properly, one can achieve greater later stage power saving though reference grouping.

C. Residue Shaping

The TSAR structure also allows for resolution improvement though residue shaping due to the three-level redundancy in a multistage ADC [22], [23]. Unlike in a binary or subradix SAR, the residue voltage after each stage of the TSAR will have a higher probability of being within the center half of the given stage's full-scale range. In other words, if the SAR has a uniform input probability density function (PDF), the width of the majority of the residue in each stage should decrease by a factor of 2 in comparison with the PDF of a binary SAR and the PDF magnitude should increase by a factor of 2, as shown in Fig. 8. Note that residue shaping works just as well with a nonuniformly distributed input PDF, but the uniform is described here for conceptual understanding. Also, the reference levels in Fig. 8 are an example configuration for illustration purposes and are not the only possible setting, as will be described later. Mathematically, this is due to the stage transfer function of the TSAR, which is

$$\mathrm{V_{OUT,STAGE}} = \begin{cases} \mathrm{V_{IN}} - \frac{\mathrm{V_{FS}}}{2}, & \text{for } \mathrm{V_{IN}} > \frac{\mathrm{V_{FS}}}{4} \\ \mathrm{V_{IN}}, & \text{for } -\frac{\mathrm{V_{FS}}}{4} < \mathrm{V_{IN}} < \frac{\mathrm{V_{FS}}}{4} \\ \mathrm{V_{IN}} + \frac{\mathrm{V_{FS}}}{2}, & \text{for } \mathrm{V_{IN}} < -\frac{\mathrm{V_{FS}}}{4} \end{cases} \tag{3}$$

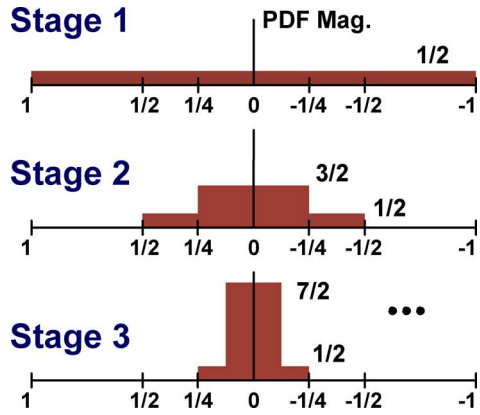

Fig. 8. Residue shaping effect illustrated by the stage residue PDF modification of the TSAR structure with quantizer thresholds at $\pm \mathrm{V_{FS}}/4$ of the stage full-scale range and for a uniformly distributed input.

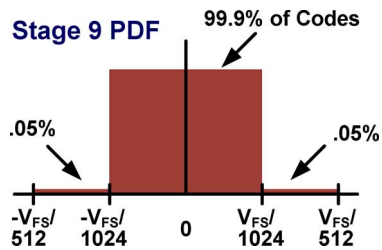

Fig. 9. PDF of last SAR stage showing codes compressed to within $\mathrm{V_{FS}}/2$ due to residue shaping with a full-scale uniformly distributed input signal.

where $\mathrm{V_{IN}}$ and $\pm \mathrm{V_{FS}}$ are the input and full-scale ranges of a given TSAR stage. This transfer function results in an input stage PDF magnitude of

$$\mathrm{PDF\,(Stage)} = \begin{cases} \frac{1}{2}, & \text{for } \mathrm{V} > \frac{\mathrm{V_{FS}}}{2} \\ 2^{(\mathrm{ST}-1)} - \frac{1}{2}, & \text{for } -\frac{\mathrm{V_{FS}}}{2} < \mathrm{V} < \frac{\mathrm{V_{FS}}}{2} \\ \frac{1}{2}, & \text{for } \mathrm{V} < -\frac{\mathrm{V_{FS}}}{2} \end{cases}. \tag{4}$$

Here, ST is used to denote the current stage. Since the magnitude of the PDF in the next stage's redundant region increases by a factor of two, for each TSAR stage with redundancy, the probability of getting a midcode is increased further, saving additional driver and switching energy over a binary SAR. Also, since this residue shaping can occur across the entire TSAR, it is shown in Fig. 9 that the last stage residue can be squeezed into half of the range of a normal binary SAR last stage. A mathematical analysis in [22] shows that the SQNR improvement possible due to full SAR residue shaping is given by

$$\begin{aligned} \Delta\mathrm{SQNR_{R-Shaped}} &= \mathrm{SQNR_{R-Shaped}} - \mathrm{SQNR_{Traditional}} \\ &= 20\log_{10}\left[2\left(1-2^{-\mathrm{ST}}\right)\right]. \end{aligned} \tag{5}$$

This results in an effective extra 6 dB of signal-to-quantization-noise ratio (SQNR) or an extra bit. In a mismatch-limited SAR, this can reduce the total capacitance by a factor of two since the capacitor spread decreases by one bit, resulting in large energy savings. In a thermal noise-limited SAR, an extra stage can be eliminated resulting in saved comparator, driver, switching, and logic energy.

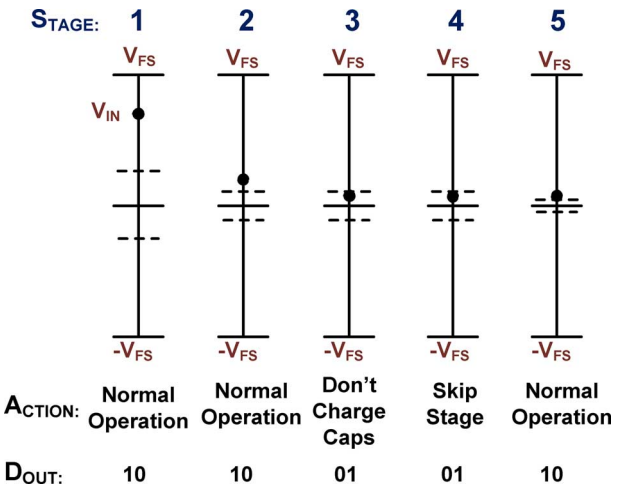

Fig. 10. Five-stage TSAR signal diagram example illustrating the effect of reference grouping on stage skipping. Stages 1 and 5 have separate redundancy thresholds while stages 2–4 all share a common threshold.

IV. TSAR Structural Enhancements

Until this point, the assumption has been made that each stage has a separate time reference level, setting a unique redundancy threshold. However, this is not optimal for a number of reasons. First, we want to minimize the number of references that have to be generated for the tine comparison (even if they are coarse). Second, we can actually save TSAR energy by grouping reference levels together.

A. Reference Grouping

In a pipelined 1.5-b/stage ADC, the redundancy levels are dictated by the ADC wide references (typically at $\pm V_{FS}/4$), meaning that the input-referred redundancy thresholds decrease by a factor of two with each stage. In the TSAR however, since there is no interstage gain, the redundancy levels must be uniquely set in each cycle. While it is possible to reset them in each phase such that they decrease by a factor of two, they can also be kept the same across multiple cycles as long as the condition that the redundancy level does not exceed the next stage's full scale range ($V_{FS}/2$ of the current stage) is met. Grouping reference levels turns out to be beneficial for the TSAR operation in that, when two stages share a common redundancy range, there is the potential to skip stages. This is illustrated in Fig. 10. Here, in the first two cycles, the input is large and positive and is outside the redundant zone. This means the output is a typical "10" code and the DAC must be switched to minimize the virtual ground voltage. In the third cycle, however, the input is in the redundant or "01" region, thus the DAC and drivers do not have to operate. In the fourth stage, since the redundancy range exactly matches that of the third stage, we deterministically know the output code will be again "01." This means there is no need to do any comparison operation or switch the DAC and drivers since the code is copied from stage three and no virtual ground movement is required. Thus, the fourth cycle can be skipped, eliminating that stage's comparator, DAC, driver, and logic power. By grouping more stages, there is the potential for additional stages to be skipped, however, the initial redundancy range decreases in the first stages of the grouping. This means that adding another stage to a large group will result in minimal energy improvement since the full-scale range of the first stage in the group will be large with comparison to the grouped redundancy range.

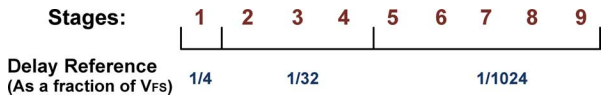

Fig. 11. TSAR prototype time reference groupings with values shown as a fraction of the full-scale input range.

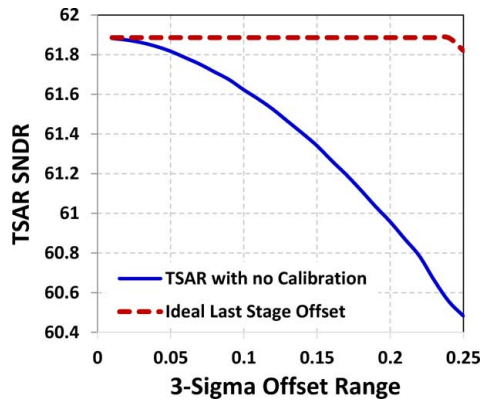

Fig. 12. Impact of sub-ADC normally distributed reference-level offsets on the overall resolution of the 10-b TSAR structure (offset distribution is plotted as a fraction of the full-scale range of the stage).

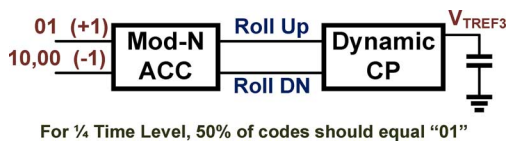

Fig. 13. On-chip statistical digital background calibration unit block diagram for time reference three.

Since the TSAR conversion delay is still determined by the worst case delay, i.e., when no skipping occurs, the stage grouping will only improve power consumption and not ADC bandwidth. In order to maximize energy saving due to grouping, it is important to see that grouping will reduce the DAC windowed switching energy savings in early stages of the group. Thus, often having small or individual reference groups for the MSB stages is important while larger groups are better for later stages where comparator energy dominates. The grouping used in the TSAR prototype is shown in Fig. 11 and was determined by running exhaustive energy simulations with block-level power data generated from simulation. Here, only three separate references are used with the first two being coarse since its accuracy has no direct impact on the resolution of the TSAR as long as they do not exceed the over-range bounds of the redundancy. The third can also be coarse, but its accuracy will determine the quantization error bound for the last bit; thus, to get a full final bit, the reference level will need to be slightly more accurate than the first two, as described in [22].

B. Time Reference Calibration

Since the last reference level controls the final bit resolution, its accuracy can only degrade the final SQNR by at most 6 dB,

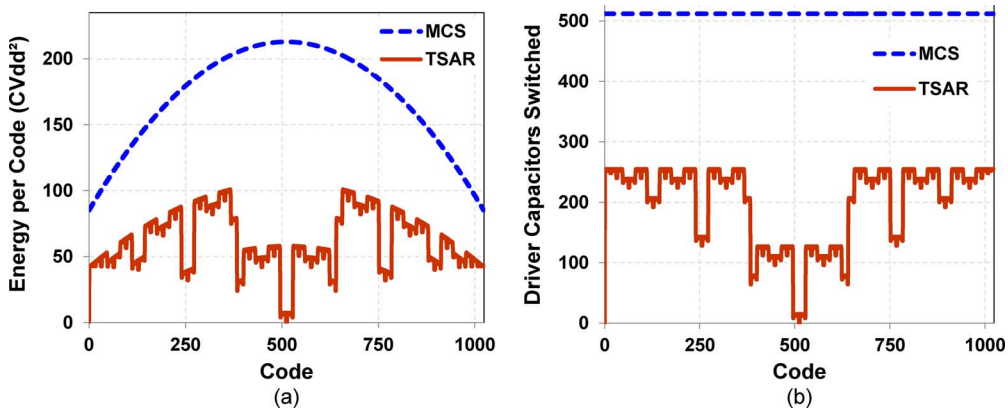

Fig. 14. TSAR DAC energy dissipation quantified in terms of (a) switching energy per code for the binary-weighted capacitive DAC-based TSAR and MCS structures in units of $C_{UNIT} * V_{DD}^2$ and (b) DAC driver energy per code for the binary capacitive DAC-based TSAR and MCS structures where one driver corresponds to a single unit capacitor.

assuming it does not cause an over-range error. Fig. 12 shows the SNDR degradation of the TSAR structure in the presence of time reference offsets distributed in the voltage domain from 0 to $V_{FS}/2$. Also shown is when the final time reference distribution is ideal (at $V_{FS}/4$). Even if the threshold is bounded to within $3V_{FS}/8$ to $3V_{FS}/16$ (1/2 typical allowed redundancy range) in the voltage domain, the 10-b resolution can be maintained with less than 1 dB of degradation, as described in [22]. These are broad reference bounds when translated to the time domain and can be reasonably set by the statistical background calibration loop shown in Fig. 13. Since the ideal final-stage reference-level sets 50% of the second-to-last-stage digital outputs to be redundant (due to residue shaping), the calibration unit accumulates the number of redundant ("01" code) events for this stage with a weight of 1 and nonredundant ("00" and "10" code) events with a weight of -1. When an accumulation rollover event occurs due to an unbalanced code output, a dynamic charge pump can increment or decrement the reference value held on a capacitor feeding a current-starved timing voltage-controlled oscillator (VCO) to adjust the time reference. This allows the final SQNR degradation due to time reference mismatch to be controlled well under 1 dB. This calibration operates in the background and counts at 1/64 the master clock rate with rollovers occurring no faster than 1/4096 the clock rate, making power consumption negligible.

C. TSAR Overall Power Savings

The implementation of the TSAR structure allows for power savings from a number of sources. The resulting power reduction can be seen by examining the total DAC switching, driver, and comparator power reduction. Switching and driver power reductions are shown per code in Fig. 14(a) and (b) *versus* the traditional MCS SAR. Here, the combined power savings come from the TSAR window function DAC activity reduction and stage skipping. In the mismatch-limited case, DAC switching and driver energy is reduced by 63.9% and 61.3%, respectively, over the MCS structure and 27.2% and 29.6%, respectively, in the thermal-noise-limited case. Fig. 15 shows comparator activity reduction due to stage skipping and residue shaping. Due to the TSAR structure, on average, 8.03 operating cycles and 6.53 DAC switching events are required for a 10-b output word with only three distinct time references. This translates to a comparator activity and power reduction of about 19.5%. Note that this is in stark contrast to other redundancy schemes, which often require up to 1.5 × more stages and can have side effects such as nonbinary arrays, digital complexity, and extra analog-domain shifting [4]–[7].

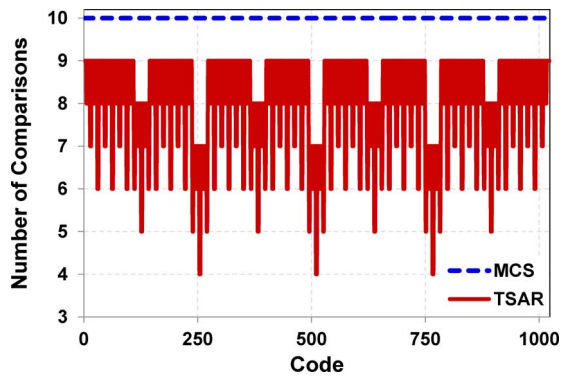

Fig. 15. Number of comparisons per code for 10-b MCS and TSAR structures where the maximum number of TSAR comparisons is nine due to PDF residue shaping (excluding top and bottom codes) and can be reduced by stage skipping.

V. TSAR Implementation

The TSAR structure shares much of the same foundation as the MCS SAR [12] with the exception of the analog core and SAR logic. The input switches are bootstrapped [24] and the DAC drivers are simple inverter-based buffers driving three-way switches for G_{ND}, V_{DD}, and V_{CM} voltages. The capacitive DAC is laid out in unit elements in a common centroid approach.

A. Quantizer Implementation

The quantizer of the TSAR consists of a high-accuracy dynamic voltage comparator followed by two time comparator units timed by a delayed clock. The voltage comparator is shown in Fig. 16 and consists of a pMOS-only latch [25] and properly sized input and clock devices for noise considerations [26], [27], tested with transient noise simulations. The output buffers contain a high-V_{TH} inverter pair to prevent comparator glitching. Following the output buffer are two matching time latches that perform the time quantization. These latches consist of a gated and buffered back-to-back inverter pair that are enabled and

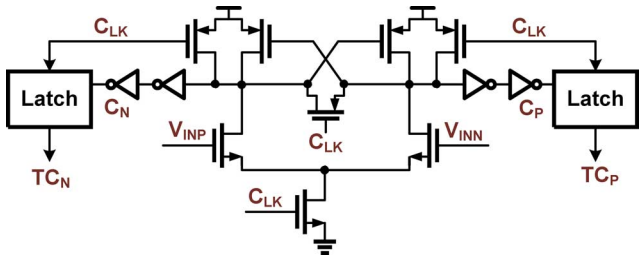

Fig. 16. TSAR quantizer implementation showing a dynamic latched comparator followed by time latches.

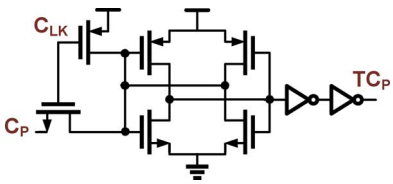

Fig. 17. Back-to-back inverter-based time latch transistor-level structure.

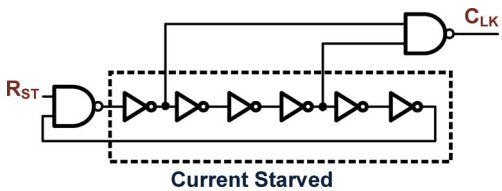

Fig. 18. Internal clocking unit generating the pulsewidth modulated clock feeding the quanitzer.

reset by the high and low states of the quantizer clock, as shown in Fig. 17. The clock of the quantizer unit is generated from a gated current-starved inverter-based VCO shown in Fig. 18.

When the clock to the quantizer rises, the voltage comparator begins regenerating, driving one output low. At the same time, the time latch becomes transparent, allowing the output of the voltage comparator to pass to the SAR logic. On the falling edge of the clock, the time latch opens and the voltage comparator is reset. If the voltage comparator output resolves to a logical "1" or "0" before the falling edge of the clock, then that data is passed thought the time latches and to the SAR, which drives the DAC during the reset phase. However, if the voltage comparator does not resolve before the falling edge of the clock, the time latch outputs no data and the SAR assigns the mid-code ("01") for that stage. Thus, the TSAR time quantizer reference is based on the pulsewidth of the clock which is modulated by the reference voltage applied to the internal clocking VCO. Once the quantizer clock falling edge arrives and the time comparator data is latched, the DAC will operate if needed and the next SAR phase will be triggered, as shown in Fig. 19. The SAR phase change will trigger a reference change if there is a reference grouping switch. This reference change will in turn control the pulsewidth of the next quantizer clock.

B. Logic Implementation

The TSAR critical path logic is similar to that of the traditional SAR structure, however contains some modifications. Typically, the SAR contains a ring counter made of flip-flops to synchronize the SAR operation and another set of latches or

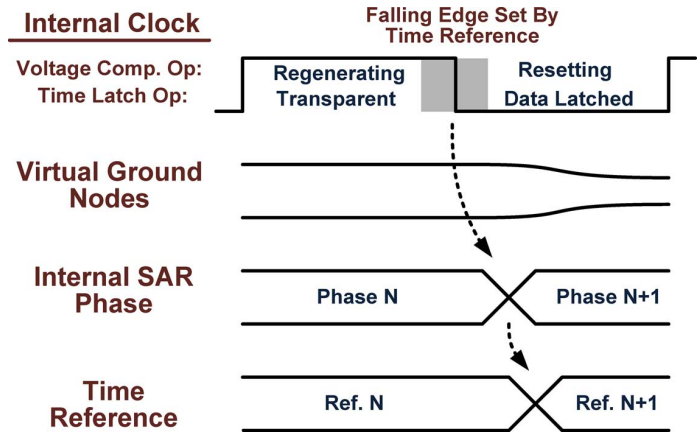

Fig. 19. TSAR prototype timing diagram showing quantizer operations and summarized logic dependencies.

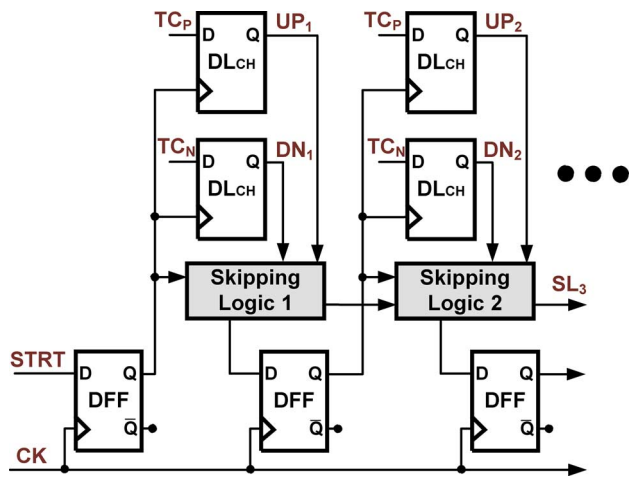

Fig. 20. State machine and data latching TSAR logic showing location of stage-skipping decision structures.

flip-flops to grab the digital data [13], [25]. In the TSAR implementation, skipping logic blocks are added, as shown in Fig. 20 in order to either enable or skip the next phase from being generated. These logic blocks examine the current cycle and digital outputs in order to enable either the next state or the first state of the next time reference grouping.

Another modification that was made is to the actual flip flops used in the state synchronization. The synchronization was provided by connecting the flip-flops as a one-hot ring counter. In order to reduce power and provide an easy reset capability, the traditional dynamic TSPC flip-flop was utilized [28], [29]. The dynamic nature of the flip-flop is not an issue since it is not in the critical timing path and setup and hold requirements were not violated. One downside of using this structure however, is that when the input is a logical zero and the clock is applied, a large amount of energy is used due to internal switching, as shown in Table I. This can be mitigated by clock gating [30] however that requires a large overhead for such a small ring. Another solution is shown in Fig. 21. Here an extra pMOS transistor is added as an internal gate when the input is low, which is the majority of the time in a SAR one-hot ring counter. With this simple modification, the dynamic power of the ring counter can be reduced by nearly 70% resulting in a significant logic power

TABLE I
TSPC FLIP-FLOP CLOCKED ENERGY PER CODE FOR THE TRADITIONAL AND PROPOSED STRUCTURE FROM 0.13-μm CMOS SIMULATION

Bit (N-1)	Bit (N)	Energy TSPC	Energy Proposed
0	0	7.93 fJ	0.10 fJ
0	1	3.73 fJ	3.67 fJ
1	0	9.10 fJ	6.69 fJ
1	1	0.02 fJ	0.02 fJ

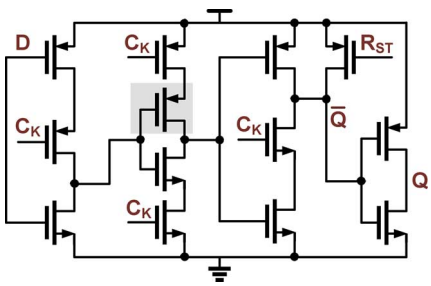

Fig. 21. Traditional TSPC flip-flop with synchronous reset and internal gating transistor for reduced one-hot ring counter power consumption.

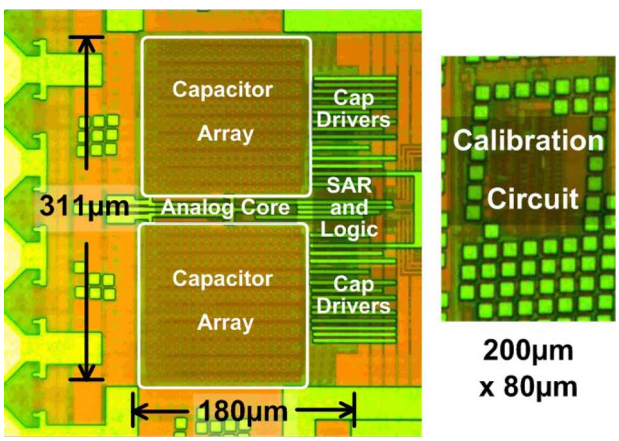

Fig. 22. TSAR micrograph showing core circuitry and calibration unit.

savings. The one downside of this modification is that the setup time is now increased by nearly 50%, but in this application, the ring counter clock will not induce a setup time violation.

C. Prototype Design

The final TSAR prototype was fabricated using 0.13-μm CMOS technology from Tower JAZZ semiconductor. The die micrograph is shown in Fig. 22, with a total active area of 0.056 mm^2. The area is dominated by the capacitive DAC which has a unit capacitor size of 15 fF chosen for matching considerations. Some traditional foreground calibration was applied to further remove static capacitor matching issues, resulting in about 2-dB total improvement. The statistical calibration unit for the third time reference is 0.016 mm^2, and this size can be reduced with the use of place and route technology (which was not available for this prototype) and digital process scaling.

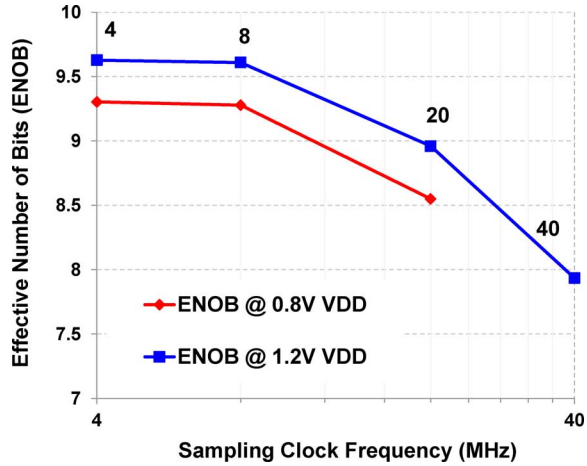

Fig. 23. TSAR ENOB *versus* sampling clock frequency for a Nyquist-rate input.

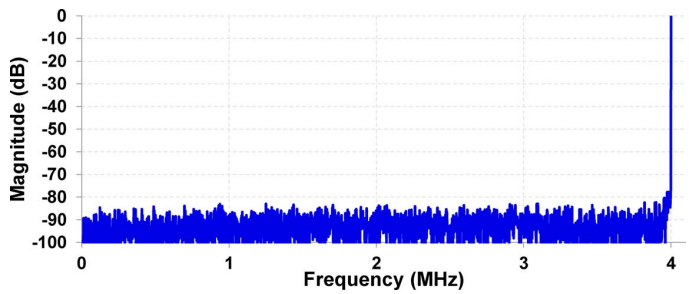

Fig. 24. 2048-point FFT of the TSAR with a sampling clock of 8 MHz and a Nyquist input signal at a supply of 0.8 V.

VI. MEASURED RESULTS

The 10-b TSAR prototype operates up to 40 MHz from supply voltages of 0.8 to 1.2 V as shown in Fig. 23. At 8 MHz and a supply of 0.8 V, the power was 83.8 μW, which, with an ENOB of 9.28, results in a figure of merit (FOM) [31] of 16.9 fJ/C-S. The frequency response at this point is shown in Fig. 24, and it can be seen that the resolution is not distortion-limited. The high-frequency degradation is due to the input path of the prototype and is not limited by the core speed since that is dictated by the internal delay-cell-based clocking of the critical path (i.e., quantizer, DAC, logic, and drivers), and is the same at low and high clock frequencies and input bandwidths. For sampling bandwidths lower then 50 MHz, the TSAR is powered down and placed in the sampling state for an extended period. A 12-b TSAR structure was also measured where an extra two bits were gained by allowing the time comparator to act as a 2-b backend flash. Here the power was not increased from the 10-b prototype since this backend resolution increase was present, but not used in the original TSAR test chip. Here, at 8 MHz and a supply of 0.8 V, the power was 75.2 μW, which, with an ENOB of 9.87, results in a FOM of 10.02 fJ/CS. The INL and DNL results are shown in Fig. 25 for the uncalibrated TSAR at a 12-b level. The INL shows the major transition points at the edges of the first-stage redundancy.

Overall power consumption of the prototype TSAR was reduced by 26% in testing by enabling the time quantization at 8 MHz. Another benefit of the TSAR structure is that the total power is related to the input magnitude, as a smaller input

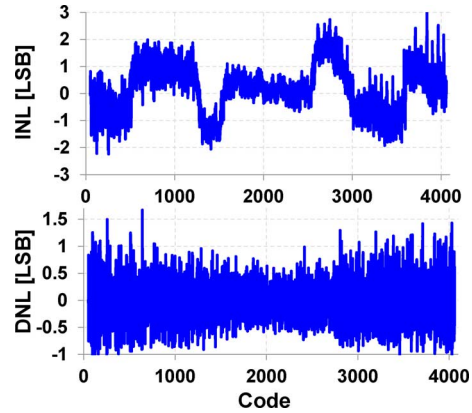

Fig. 25. INL and DNL plots at a 12-b level and with no foreground calibration.

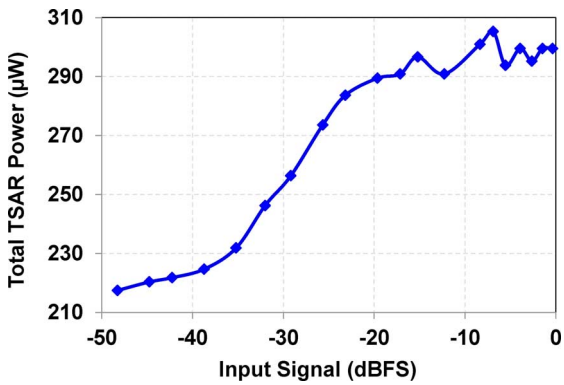

Fig. 26. Total TSAR power consumption versus input signal magnitude at a supply of 1.2 V and clock frequency of 8 MHz.

TABLE II
TSAR MEASURED RESULTS FOR BOTH THE 10-b AND 12-b REVISION PROTOTYPES WITH COMPARISONS TO OTHER REFERENCED S TATE-OF-THE-ART SAR STRUCTURES

Specification	TSAR	TSAR	TSAR + BE	JSSC 2010 [13]	VLSI 2010 [3]	JSCC 2011 [7]	JSSC 2010 [11]
Architecture	SAR	SAR	SAR	SAR	SAR	SAR	SAR
Technology	0.13µ	0.13µ	0.13µ	90n	0.18µ	0.13µ	0.13µ
Sampling Rate (MS/s)	8	20	8	100	10	40	50
Supply (V)	0.8	1.2	0.8	1.2	1.0	1.2	1.2
ENOB	9.27	8.96	9.87	8.6	9.83	8.11	9.18
SFDR (dB)	76	78	79	71	69	58	62
Power (uW)	83.8	526	75.2	3000	98	550	826
Area (mm²)	0.056	0.056	0.056	0.18	0.086	0.32	0.052
FOM (fJ/CS)	16.9	52.8	10.0	77	11	50	29

signals results in a higher probability of early stage redundancy. Fig. 26 shows the total TSAR power consumption *versus* the input magnitude demonstrating a power reduction of about 30% for small magnitude signals. This makes the architecture a good choice for signals that are normally quiet but have sparse transient inputs. Furthermore, the time threshold levels can be modified for lower power in the presence of small inputs. The power consumption of the SAR is dominated by the DAC and comparator blocks. From simulation, the DAC (capacitors and drivers) consume 40% of the total power with the fine voltage comparator taking 38%. Since the time comparator structure is simple and sized for lower accuracy, it only consumes 6% of the total overall power. The remaining 16% of the power is consumed by the digital logic and clocking circuitry. Measurement results are summarized in Table II for various supply and clocking configurations. Here, for the TSAR, the ENOB is measured for an input equal to $fs/2$ and the FOM is defined as $\text{Power}/[2^{\text{ENOB}}(fs)]$.

VII. CONCLUSION

This paper has proposed a ternary SAR (TSAR) ADC with sub-ADC decision time quantization. The TSAR structure examines the transient information of the voltage comparator regeneration in a traditional SAR loop to provide increased performance. Improvements include enhanced accuracy through redundancy, residue shaping, and statistical calibration, increased speed though reduced comparator delays and capacitor settling time, and reduced power consumption though stage skipping, DAC activity reduction, and logic modifications. Switching and driver energy were both reduced by about 60%, and comparator activity was reduced by about 20%. This idea was demonstrated though a prototype implementation in 0.13-μm CMOS with an FOM of 16.9 fJ/C-S for the 10-b TSAR and 10.0 fJ/C-S for the 12-b structure.

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