Ternary R2R DAC design for improved energy efficiency

J. Guerber, H. Venkatram, M. Gande and U. Moon

An R2R DAC using three digital input levels rather than two is proposed as well as a modified two-level structure that emulates the three-level DAC's benefits. This three-level structure provides power reductions of 79% and linearity improvements due to matching of a factor of 2 over the two-level case. Ideal implementation is also described in terms of the logic needed to code the DAC and the requirements of the additional third reference level.

Introduction: Digital-to-analogue converters (DACs) are ubiquitous in modern devices for the translation of digital data into real-world signals. One variety, the R2R DAC, has wide use in applications ranging from sensors, digital waveform generation, and general purpose mid-speed and high accuracy DACs [1–3]. R2R circuits can also be used along with thermometer DACs to make segmented structures, or be inverted for current mode operation [4].

Typically, a voltage mode R2R DAC is designed as shown in Fig. 1, with a series of R and 2R segments and two-level digital codes on the segment inputs. As the segments move away from the output node, the impact of the digital code on the output voltage decreases by a factor of 2 in each stage. The power consumed in this DAC is then determined not by the magnitude of the output, but by the number of unit segments that are switched in opposite directions and their proximity to each other. For example, the digital code 111000 would burn more static power than the 110000 code, but much less static DAC power than the code 101010 owing to the interleaving of the supply and ground connected resistive segments. This is because there is a high current path from all the VDD connected resistors in 101010 but in 110000, the current from the first stage is mitigated by the node voltage boost provided by the second stage. Also, connecting this DAC differentially will burn on average double the power.
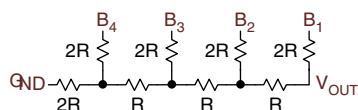

Fig. 1 *Traditional 4b binary R2R DAC circuit (B1 is the MSB)*

Ternary R2R DAC: One alternative to the traditional binary R2R structure for reduced power consumption in differential operation is the ternary R2R DAC shown in Fig. 2, which has a similar three-level reference selection to [4] and [5]. Here, each digital input to the DAC {T1, T2, T3 …} can take a level of the set {GND, VCM, VDD} whereas the binary DAC could only take the levels {GND, VDD}. This architecture can burn less power than the two-level R2R due to the reduction in voltage magnitude across segments of the DAC and the ability to reduce the interleaving code transitions (101010) with three supply levels. The implication is then that by appropriately selecting when to use the VCM level in the DAC, the energy of the overall structure can be reduced.
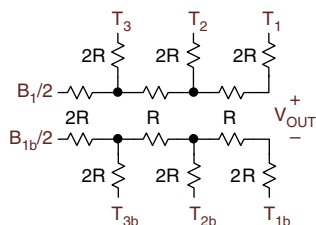

Fig. 2 *Proposed three-level 4b ternary R2R DAC (shown differentially)*

The optimal three-level switching scheme can be arrived at by making a couple of observations. First, the lowest power DAC coding is when the inputs are all the same code, either all VDD, GND, or VCM. Secondly, the net current into VCM is zero due to the differential nature of the circuit. Thus, the optimal coding should maximise the time that VCM is connected to a segment of the DAC (minimising

the number of supply connections). To do this we need a binary to ternary coding shown in Fig. 3. This coding operation is implemented by the logical function:

$$T_{N(VDD)} = (B_1)(B_{N+1}) \qquad (1)$$

The function is ANDing the first and current digital binary code to determine the optimal ternary DAC level. Notice that this operation does not change the output voltage of the final conversion except for adding an LSB/2 offset to the positive and negative codes. This can be corrected for by adding the same offset back (B1/2) to the R2R as shown in Fig. 2. Also, this coding scheme reduces the total number of stages in the R2R by replacing the information from the first binary bit with the switching of DAC supply.

Fig. 3 *Encoding table for three-level R2R DAC (left) and logic for three-level DAC (right)*

Modified two-level R2R DAC: In the preceding Section, the power consumption of the traditional R2R DAC was reduced by adding a middle code to mitigate the effect of alternating supply referenced codes on the binary DAC inputs. This same effect can be emulated with only two levels differentially as shown in Fig. 4. Here, assuming the DAC is fully balanced around the middle of the supply, the VCM switching events can be replaced by simply shorting the two sides of the respective R2R stages together. To ensure balancing and maintain only two reference levels, either the binary first bit and its inverse should be used on the ends of the DAC or complementary supplies. Adding complementary supplies as shown in Fig. 4, results in an offset that can be corrected by shifting the digital bits coming into the DAC. While this DAC outputs the same codes as the previous three-level DAC (with an offset), the settling time can be worse due to sampling transients on the input nodes for sharing events, but this could be minimised by connecting all the shorting nodes together (since they should only ideally be at a potential of VCM).
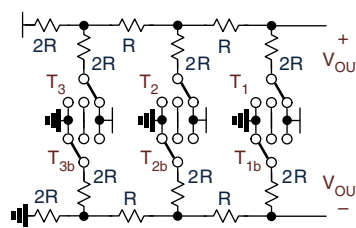

Fig. 4 *Modified two-level 4b differential R2R DAC*

DAC energy and linearity comparison: To understand the energy difference between the two-level and three-level R2R structures (here the modified two-level has the same energy profile as the three-level), the normalised static power per code is shown in Fig. 5 for a 6b R2R differential example (ignoring switch resistance). The power of the ternary R2R is improved by nearly 79% for a uniform input PDF and the power for each individual code is reduced. The peaks and troughs in both the plots correspond to the high power codes when there are many interleaved digital codes on the DAC inputs and the low power events when there is a string of the same code across some portion of the DAC. The power in both cases does not go to zero when the inputs are all the same potential due to the current through the last R2R stage in the differential configuration.
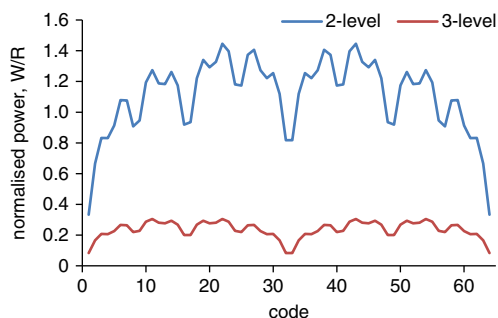
Fig. 5 *Normalised power per code for 6-bit example differential two-level and three-level R2R DACs*

In addition to the power, the static linearity, measured by the DAC's INL, improves by a factor of 2 based on the addition of an extra reference level to the output. This is because in the binary R2R DAC, there could be a large DNL event (code jump) between the 1000… and 0111… middle codes since all of the resistors are changing their supply references between the two events. In the three-level case though, the middle transition is when all the DAC inputs are VCM, except the switching last stage, meaning the code jump due to mismatch in the resistive elements is small. The major code transition is then moved to a quarter of the full scale range. This result is similar to that of three-level capacitive DACs as in [6].

When implementing the three-level structure, it should be mentioned that the net current from VCM is always 0 due to the differential nature, thus much more relaxed regulators could be used for this reference (even the transient switching events should be complementary). Additionally, the R2R structure could be implanted in a single end fashion with significant power savings, but the VCM reference would then source and sink current.

Conclusion: An R2R DAC using three digital input levels rather than two has been shown. The power of this proposed DAC is reduced by nearly 79% and the worst-case static linearity due to device mismatches is improved by a factor of 2. The additional reference used in the design sources no net current differentially and low-complexity logic for coding that DAC has been shown. Also, a modified two-level structure has been proposed that can emulate the energy reduction benefits of the three-level R2R structure.

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