Blind Background Calibration of Harmonic Distortion Based on Selective Sampling

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***Abstract*—This paper proposes a blind calibration algorithm for suppressing harmonic distortion in analog to digital converters (ADCs). The proposed algorithm does not need any external calibration signal and is first of its kind. The proposed algorithm relies on the properties of downsampling and orthogonality of sinusoidal signals to estimate the harmonic distortion coefficients. The algorithm can be operated in both foreground and background modes to remove even and odd harmonics simultaneously. The algorithm is demonstrated on a first-order ring oscillator based $\Delta\Sigma$ ADC, whose performance is harmonic distortion limited. Built in 0.13μm, the algorithm improves the SNDR of the ADC by 39dB while improving SFDR by 45 dB.**

I. Introduction

Modern day CMOS processes are characterized by scaling in terms of geometries and supply voltages. Scaling happens with digital design in perspective, thereby complicating the design of high-resolution, high-performance ADCs. Shrinking geometries tend to reduce the intrinsic gain of MOS transistors, making it difficult to realize high DC gain, wide bandwidth amplifiers. This complicates the design of high performance ADCs. To counter this problem, ADCs which are more digital in nature are being favored in smaller geometry processes. Successive approximation ADCs (SAR) [1] and digitally calibrated ADCs fit the bill perfectly [2]–[6]. In this paper, we focus on ADCs which make use of digital processing to make up for analog imperfections.

Power, linearity, bandwidth, area and process form a complex trade-off in ADC design. For example, amplifier non-linearity and capacitor mismatches in pipeline ADCs [3], capacitor mismatches in SAR ADCs [1], amplifier non-linearity, quantizer non-linearity and DAC non-linearity in $\Delta\Sigma$ ADCs lead to harmonic distortion in ADCs. These issues can be resolved in analog or digital domain. Analog domain solutions for the above issues include using larger capacitors for better matching or high loop gain, wide bandwidth and low distortion amplifiers or using feedback loops, which unfortunately are power intensive and are also becoming increasingly difficult to design in modern day CMOS process.

On the other hand, reduced gate delays and ease of portability across processes make digital calibration for analog imperfections very attractive in modern day CMOS processes. However, there are only a handful of digital calibration techniques which can remove harmonic distortion in ADCs. [1]–[6] provide a few alternatives for removing harmonic distortion in ADCs but have their own limitations, as shown in Table I. This paper proposes a, first of its kind, blind calibration algorithm, which can operate in both foreground and background modes, to remove harmonic distortion in ADCs. The proposed algorithm does not use any external calibration signal and only uses the properties of downsampling and orthogonality of sinusoidal waves to calibrate for harmonic distortion in ADCs, hence the blind nature of it.

TABLE I
Comparison with existing architectures

Reference	Notes
[1]	Calibration performed in software. Uses two ADC paths with dithered test signal. Calibration demonstrated only for odd harmonics.
[2]	Calibration performed on chip. Uses multiple pseudo-random external sequence.
[3]	Similar to structure in [2]. Implemented on a pipeline ADC.
[4]	Corrects non-linearity of only one stage using a binary random number generator. Assumes ideal back-end ADC.
[5]	Needs an external input. Normal operation of ADC is interrupted and missing sample is interpolated.
[6]	Requires a 13-bit accurate signal for calibration. Needs to be clocked at higher frequency as compared to ADC rate.
This Work	Requires no external calibration signal. Can operate in background and removes multiple harmonics simultaneously.

Sections II explains the background for the algorithm and illustrates the working of the algorithm in a single harmonic case in a foreground mode. Section III illustrates how the algorithm can be extended to operate in background mode. In section IV, the algorithm is extended to calibrate for multiple harmonics simultaneously. Section V briefly describes the implemented VCO based first order $\Delta\Sigma$ ADC, with section VI describing the final architecture. Measurement results are presented in section VII, with the paper being concluded in section VIII.

II. Proposed Algorithm

Figure 1 shows the single tone frequency response of an ideal ADC and non-ideal ADC which has third harmonic distortion only. As shown, when a sinusoid (of frequency f_{in}) is given to an ideal ADC, the frequency spectrum of its digital output (D_1) consists of a single tone at f_{in}. When

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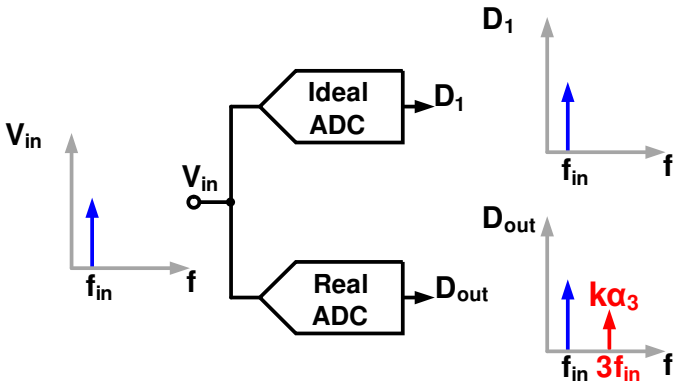


Fig. 1. Single tone frequency response of ideal and non-ideal ADC.

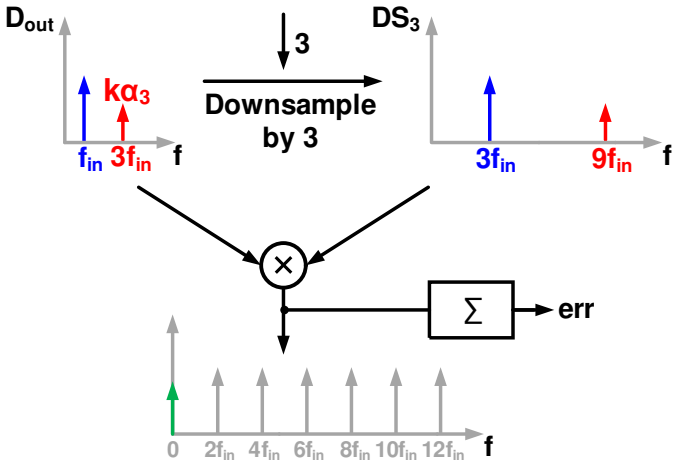


Fig. 2. 3^{rd} harmonic extraction.

the same input is given to a non-ideal ADC which suffers from third harmonic distortion, the output (D_{out}) contains a tone at f_{in} and additional harmonic distortion component at $3f_{in}$. The assumption that the non-ideal ADC suffers only from third harmonic distortion is for simplicity reasons only. This algorithm is not limited to single harmonic tones.

For the remainder of this section, the coefficient of distortion is assumed to be α_3. Therefore, the magnitude of harmonic distortion tone at $3f_{in}$ is proportional to α_3 (kα_3). The non-ideal ADC is modeled as follows:

$$D_{out} = D(V_{in}) + \alpha_3 \times D(V_{in}^3) \tag{1}$$

Where D_{out} is the output of the non-ideal ADC, and $D(V_{in})$ is the ideal digital representation of V_{in}. In the above setup, the source of distortion is not important i.e. the distortion could be due to any component in the entire system.

The proposed algorithm relies on two important signal properties (1) Downsampling and (2) Orthogonality of sinusoidal waves.

A. Downsampling

Downsampling is the process of reducing the sampling rate of a signal. In time domain downsampling leads to dropping of

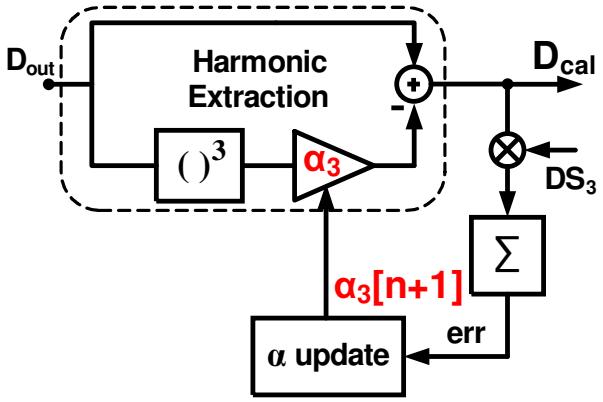


Fig. 3. LMS engine.

samples, whereas in frequency domain downsampling leads to input spectrum being spread out. Figure 2 shows the frequency spectrum of output of ADC (D_{out}) and the spectrum obtained after downsampling by 3 (DS_3). The original spectrum of D_{out} has tones at f_{in} and $3f_{in}$, while the downsampled spectrum has tones at $3f_{in}$ and $9f_{in}$. Note that $3f_{in}$ tone in D_{out} and $9f_{in}$ tone in DS_3 are due to the harmonic distortion in the ADC.

B. Orthogonality

A key property of sinusoidal waves is that they are orthogonal at different frequencies. In other words, the sum of product of two sinusoids is zero if the two frequencies are different and is non-zero if the frequencies are same. i.e.

$$\sum_{n=1}^{N} sin(f_1 n) \times sin(f_2 n) = \begin{cases} 0 & \text{if } f_1 \neq f_2, \\ \neq 0 & \text{if } f_1 = f_2 \end{cases} \tag{2}$$

An alternative way of looking at the above property is that the product of two sinusoids of same frequencies has a component at DC, while product of two sinusoids of different frequencies does not have any component at DC. Therefore, obtaining a non-zero average for a product of two sequences implies that the both the signals have a common frequency term in it.

C. Proposed Algorithm

Combing the properties of downsampling and orthogonality of sinusoid waves, the coefficient of third harmonic distortion (α_3) is estimated. This is done by taking the running average of the product of the two digital bit streams D_{out} and DS_3. As shown in Fig. 2 when there is harmonic distortion present in the ADC, the running sum of product of D_{out} and DS_3 has a component at DC, whose magnitude is proportional to α_3. Using this information, the third harmonic distortion term can be extracted using an LMS based engine. The updated error term of the LMS engine is given as

$$err = \sum (D_{cal}[n] \times DS_3[n]) \tag{3}$$

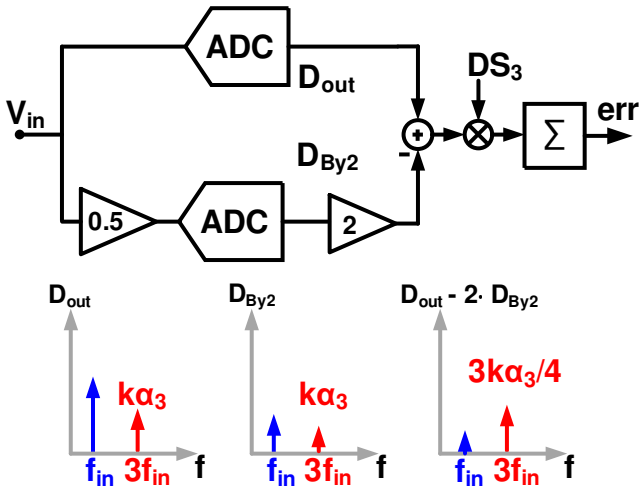


Fig. 4. Background implementation.

Therefore the error term is zero if and only if the calibrated output D_{cal} and the downsampled output DS_3 do not have any common sinusoid in their digital streams. The simplified update equations for the LMS engine are given in equation 4 which is also illustrated in Fig. 3.

$$D_{cal}[n+1] = D_{out}[n] - \alpha_3[n] \times D^3_{out}[n], \quad (4a)$$

$$\alpha_3[n+1] = \alpha_3[n] + \mu \times err \quad (4b)$$

III. Background Calibration

The algorithm discussed so far needs a clean sinusoid input and can be operated in a foreground fashion. The above algorithm can be made to operate in a background mode by removing the signal component from the output digital stream and dealing only with the harmonics. As shown in Fig. 4, this is done by splitting the original ADC into two parts and applying input V_{in} to one ADC and an approximately scaled version of V_{in} (e.g. V_{in}/2) to the other. By doing so, the linear component of the input is scaled by a linear factor, whereas the harmonic distortion part is scaled by a different factor. Therefore, the digital stream D_{out} - $2D_{By2}$ does not have any input component present in it, but only has the harmonic distortion terms present in it. Therefore, by taking the average of the product of the above obtained stream and the downsampled stream (DS_3), the third harmonic distortion coefficient can be estimated. The finite accuracy of the scaling by 2, in this example, is also merged into the LMS engine.

IV. Calibration for Multiple Harmonics

The above algorithm can be extended to calibrate for multiple harmonics. This is done by using multiple digital output streams, which are created by downsampling the output stream by the harmonic to be estimated, and then performing the above operation in unison. For example, if the ADC suffers from both k_1 and k_2 harmonic distortion, two new digital streams (1) Digital stream downsampled by k_1 (D_{k1}) and (2) digital stream downsampled by k_2 (D_{k2}) are created. The

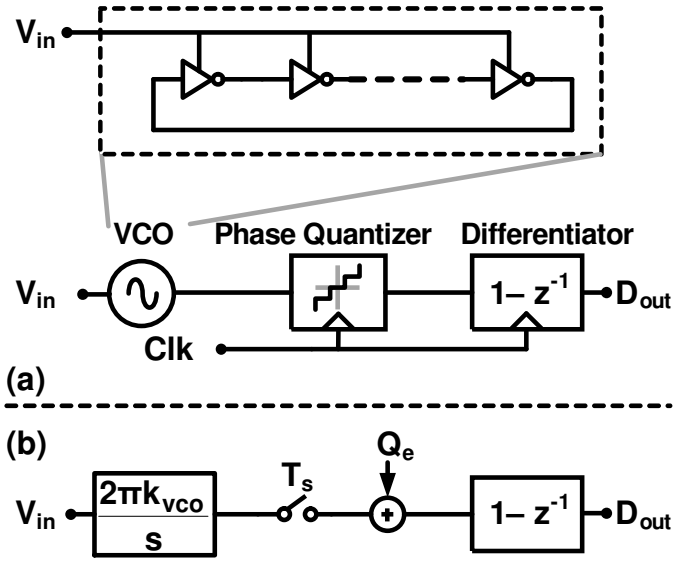


Fig. 5. (a)VCO based first order ΔΣ ADC. (b) Equivalent model.

product of the sequences D and D_{k1} gives a term proportional to k_1, whereas the product of the terms D and D_{k2} gives a term proportional to k_2. Note that the estimation of both the coefficients happens simultaneously, i.e. the modified update equation is

$$D_{cal}[n+1] = D_{out}[n] - \alpha_{k1} \times D^{k1}_{out}[n] - \alpha_{k2} \times D^{k2}_{out}[n] \quad (5)$$

The final calibrated sequence is given by

$$D_{cal} = D_{out} - \alpha_{k1} \times D^{k1}_{out} - \alpha_{k2} \times D^{k2}_{out} \quad (6)$$

V. VCO Based ΔΣ ADC

Voltage controlled oscillators (VCOs) are highly non-linear circuit elements which convert voltage information into phase. Any ADC built using VCO suffers from harmonic distortion, thereby making it an ideal candidate to test our proposed algorithm. Figure 5, shows a stand alone VCO which is reconfigured to operate as a first order ΔΣ ADC [2].

The VCO is a 15-cell ring oscillator built using standard cell inverter blocks. The supply of the inverter cells is directly controlled by the input of the system, thereby making it a supply controlled VCO. Also, most of the cells used in the design are standard cell blocks, thereby making the design highly scalable with modern day CMOS processes.

VI. Final System Architecture

Figure 6 shows the final architecture of the complete ADC. The ADC consists of two VCOs with input to the first VCO being V_{in} and the input to the second VCO being V_{in}/2. The digital outputs from the ADCs are then sent to the calibration engine, which are used to estimate the harmonic distortion coefficients, in this case 2^{nd} and 3^{rd} harmonic coefficients. Once the coefficients are estimated, the coefficients are stored in memory. The ADC now returns to normal operation, and the output of the ADC is corrected for harmonic distortion using

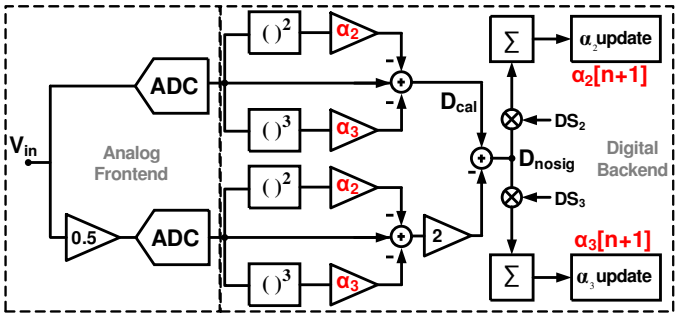


Fig. 6. Final architecture.

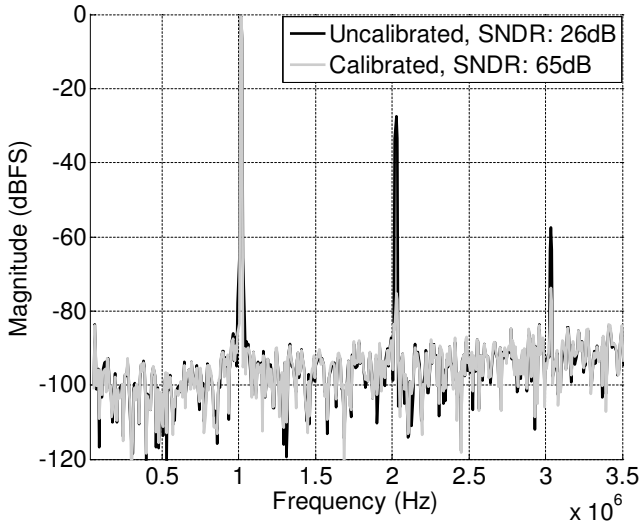


Fig. 7. Measured spectrum before and after calibration.

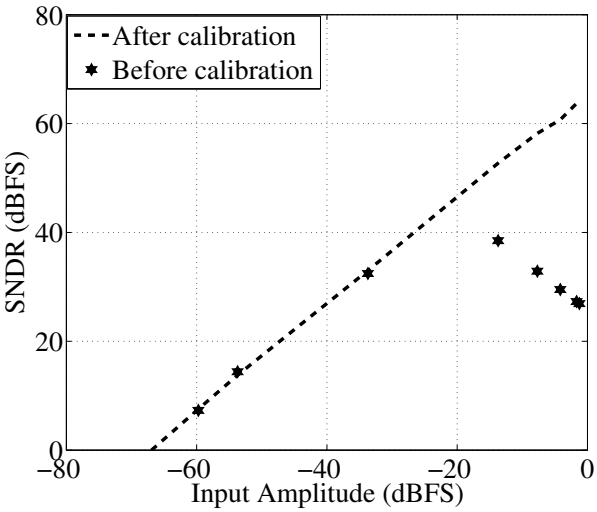
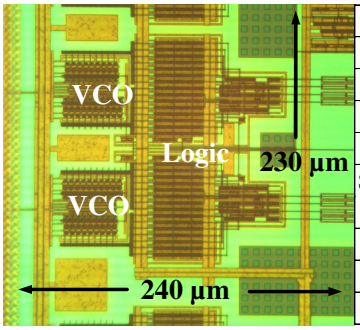


Fig. 8. SNDR vs. input amplitude.



Performance Summary		
Technology(CMOS)		0.13µm
Supply Voltage		1.2
Sampling rate		450 MHz
Signal Bandwidth		3.51 MHz
SNDR	Before Calib.	26 dB
	After Calib.	65 dB
Power		1.65 mW
Area		0.055 mm^2
FOM		162 fJ/C-S

Fig. 9. Chip micrograph and performance summary.

eq. (6). The digital engine is operated using 15-bit precision words and is implemented off-chip in software.

VII. Measured Results

The performance of VCO based first-order $\Delta\Sigma$ ADC is harmonic distortion limited, thereby making it an ideal candidate for the proposed algorithm. The prototype ADC was built in $0.13\mu m$ CMOS and occupies an area of $0.055mm^2$. The ADC operates at sampling frequency of 450MHz with an OSR of 64, resulting in a signal bandwidth of 3.51MHz. A rounded square wave signal (i.e. an arbitrary signal) is given as the input and the second and third harmonic distortion coefficients are estimated. The non-linearity correction is then performed using the above obtained coefficients.

Figure 7 shows the output spectrum for a 1MHz sinusoid input before and after calibration. Before calibration, the SNDR of the ADC is harmonic distortion limited and equal to 26dB SNDR and after calibration, the SNDR is 65dB. The power consumption of this ADC was 1.65mW resulting in an FOM of 161 fJ/C-S. The limited FOM is due to a design oversight and can be improved easily. Figure 8 shows the SNDR vs. input amplitude for the ADC. The die photo and the performance summary of the ADC are shown in Fig. 9.

VIII. Conclusion

This paper proposes a blind calibration algorithm which can be used to reduce harmonic distortion in ADCs. The proposed algorithm can be applied to any ADC architecture in general, and can be used to remove both even and odd harmonics. The successful operation of the algorithm was demonstrated for a VCO based first order $\Delta\Sigma$ ADC.

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