Analysis of Back-end Flash in a 1.5b/stage Pipelined ADC

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***Abstract*—An analysis of the impact of last stage flash in a conventional pipeline ADC is performed in this paper. The performance of a pipeline ADC can be altered significantly by calibrating the comparators in the back-end flash. Also, realizing that the input to the back-end flash (in a pipeline ADC) is not uniformly distributed,this paper proposes alternative back-end flash references to improve the overall performance of the ADC. An analysis of the performance of the pipeline with large offsets in the MDAC stages is also presented in this paper.**

I. Introduction

In the age of scaling where achieving high accuracy components becomes increasingly difficult, employing redundancy is a very attractive option. This option is increasingly observed in pipeline and SAR ADCs. In a multi-bit/stage pipeline ADC, redundancy helps to relax the offsets permissable in the flash used in sub-ADC (used in every MDAC stage) [1], whereas in a SAR ADC, redundancy helps in dealing with incomplete settling [2]. For example, in a 1.5b/Stage pipeline ADC, redundancy allows for the thresholds in a sub-ADC to only be as accurate as the current stage i.e. offsets as large as $V_{ref}/4$ can be tolerated in the sub-ADCs. Even more importantly, this offset allowed is not dependent on the total resolution of the pipeline ADC. Redundancy also provides other benefits such as allowing for PN based radix calibration [3]. The back-end of a pipeline ADC is a flash, as there is no need to amplify the residue after the final quantization [4]. The purpose of this paper is to examine the threshold levels of this back-end flash and its impact on the performance of the overall pipeline ADC. This paper also analyzes the input to the back-end flash ADC and proposes an optimized back end quantizer. The optimized quantizer can be used to reduce the number of comparators or to achieve 6dB higher resolution when compared to a traditional back-end flash designs.

Without loss in generality, we carry out the discussions for a regular pipeline ADC with 1.5b/stage MDACs with a flash ADC at its back-end. Section 2 analyzes the different threshold levels of the back-end flash in a conventional 1.5b/stage pipeline ADC and also the input characteristics of the back-end flash. Based on this, a modified back-end flash is proposed in this section. Section 3 compares the performances of the proposed architecture and the conventional architecture in practical situations, with the conclusion presented in Section 4.

II. Conventional pipeline back-end

A regular pipeline ADC consists of MDAC stages stacked one after the other with the output of Stage 'i' being the input for Stage 'i+1'. At the end of the MDAC stages, a back-end ADC (typically a flash) acts on the quantization error of the last MDAC stage. This generic architecture is shown in Fig. 1.

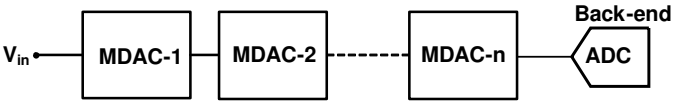

Fig. 1. Conventional Pipeline ADC

The most commonly used MDAC is the 1.5 b/stage MDAC, which resolves 3 levels/stage. The 1.5 b/stage MDAC uses two comparators in the sub-ADC, and the threshold voltages of these comparators are offset by LSB/2. i.e. the threshold voltages are $\pm V_{ref}/4$. An MDAC stage has three main blocks: sub-ADC, DAC and a gain block. The operation of MDAC is shown in Fig. 2.

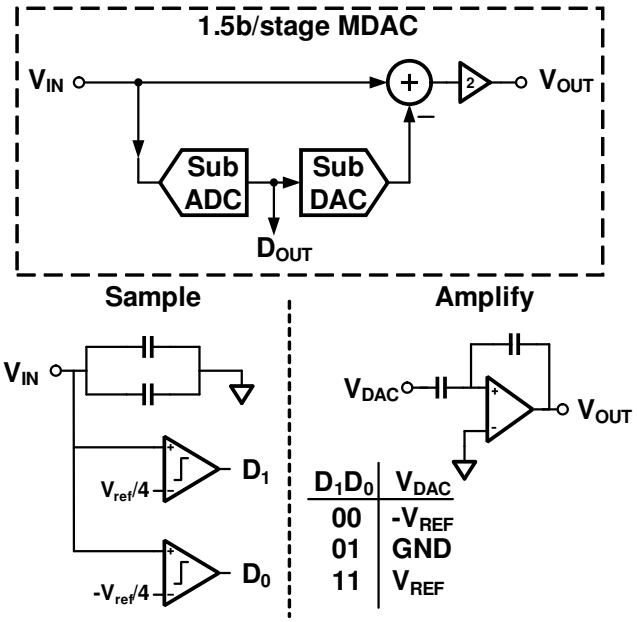

Fig. 2. 1.5 b/stage MDAC

The MDAC operates in two phases: (1) Sampling: In this phase the input is sampled on two capacitors and it is also sampled by the sub-ADC (two comparators), which gives out the digital word D_1D_0 by the end of this phase. And phase (2) is for amplification, where the signal is amplified by two,

and the corresponding DAC voltage (V_{dac}) is subtracted from the input.

The threshold voltages of the sub-ADC in the MDAC are offset by LSB/2. Whereas, the threshold for the back-end flash is typically not offset, so that it could act as an ideal back-end ADC. Therefore in this case if the back-end flash is 2-bit, then the references of the flash would be $-V_{ref}/2, 0, +V_{ref}/2$.

A disadvantage with using the above back-end flash is that an alternative reference voltage needs to be sent onto the chip ($\pm V_{ref}/2$). So instead of using the above thresholds for the back-end flash, its threshold values could also be moved by LSB/2, i.e. have reference voltages of $-V_{ref}/4, +V_{ref}/4, +3V_{ref}/4$ for the flash. The performance change due to using the modified flash is less than 0.5 dB. This is because, in the modified case, we would only have a small reduction in the dynamic range of the ADC.

The above claim can be verified by considering the distribution of the input to the back-end flash. A sinusoidal input, with peak amplitude close to V_{ref} is sent as an input to a 10-bit pipeline ADC (V_{ref} is assumed to be reference voltage of the pipeline). The pipeline ADC consists of 8x1.5b/stage MDACs and a 2-bit back-end flash ADC. The input to the first MDAC and the input to back-end flash are shown in Fig. 3

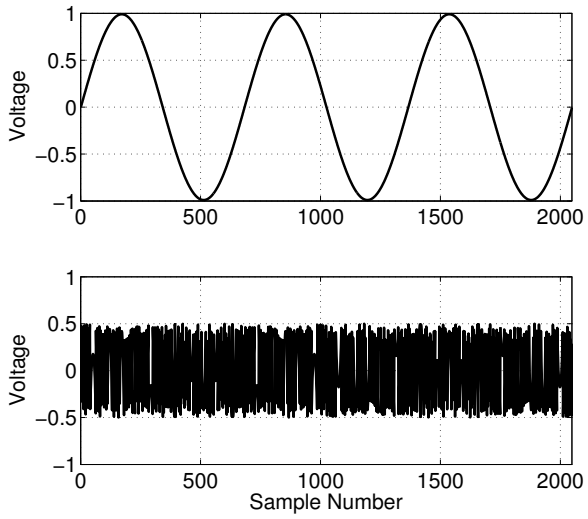

Fig. 3. Input to first MDAC and last-stage flash

Fig. 3 shows that most of the input to the back-end flash is concentrated between $-V_{ref}/2$ and $V_{ref}/2$ (where $V_{ref} = 1$), even though the input to the first MDAC varies between $-V_{ref}$ and V_{ref}. The only time when the input to the back-end lies above this range can be shown to be when the input to the pipeline is very close to $\pm V_{ref}$. Therefore, in a traditional pipeline ADC with back-end references of $-V_{ref}/2, 0, V_{ref}/2$ and input slightly less than full-scale, only the middle comparator is used. The extreme two comparators ($\pm V_{ref}/2$) are never used. Therefore, if you instead use the offset threshold voltages ($-V_{ref}/4, +V_{ref}/4, +3V_{ref}/4$), it would in effect look like a 3 level comparator (since the top most comparator $, +3V_{ref}/4$ is never used). As a result the performance of the pipeline with either of the back-end, ($-V_{ref}/2, 0, V_{ref}$) or ($-V_{ref}/4, +V_{ref}/4, +3V_{ref}/4$), is equivalent.

From the above argument, it was observed that input to the back-end flash is concentrated between $-V_{ref}/2$ and $V_{ref}/2$. This phenomenon is due to residue shaping of quantization noise as it propagates through the input chain of the pipeline ADC [5]. From the above observation, it can be concluded that only one comparator is needed in the back-end flash to limit the quantization error to $V_{ref}/2$ and hence act like a 2-bit flash. In other words, using a flash with a single comparator with a reference of "0" is equivalent to using a 2-bit flash with references of $-V_{ref}/2, 0, V_{ref}$ when the input is restricted to lie between $-V_{ref}/2$ and $V_{ref}/2$.

From the above discussion, it can also be noted that using the references of $-V_{ref}/4, 0, +V_{ref}/4$ would make the back-end flash look like a 3-bit flash, and hence make the overall pipeline look like a 11-bit ADC. In all the above architectures, the gain of the back-end flash needs to be chosen appropriately. Table I summarizes the performance for different back-end flash stages when a 8x1.5b/stage MDAC is used in the front-end.

TABLE I
PERFORMANCE FOR DIFFERENT BACK-END FLASH

Back-end flash References	SNR	# of comparators
$-V_{ref}/2, 0, V_{ref}/2$	62 dB	3
$-V_{ref}/4, V_{ref}/4, 3V_{ref}/4$	62 dB	3
0	62 dB	1
$-V_{ref}/4, 0, V_{ref}/4$	68 dB	3

Table I confirms that the performance of the pipeline ADC is the same in the first three cases and hence it is beneficial to use a single comparator at a reference of zero instead of the traditional back-end flash. For the above data, it was assumed that the MDACs where ideal and there are no offsets present in the sub-ADCs of the MDAC. However, in practice, that is not the case and offsets are present in all the sub-ADCs as well as the back-end flash. The next section discusses the performance of the different architectures in the presence of offsets.

III. OFFSETS IN A PIPELINE ADC

Up until now, the sub-ADCs of the MDACs were assumed to be ideal with no offsets present. Fig. 3 shows that the input to the quantizer lies between $-V_{ref}/2$ and $V_{ref}/2$ when all the MDACs are ideal. However, in a more practical case with offsets present in all the MDACs, the input to the quantizer would no longer be bounded between $\pm V_{ref}/2$. Fig. 4 shows the input to the quantizer in one of the practical cases when the offsets in the MDACs are varied randomly between $-V_{ref}/5$ and $V_{ref}/5$ (using a uniform distribution).

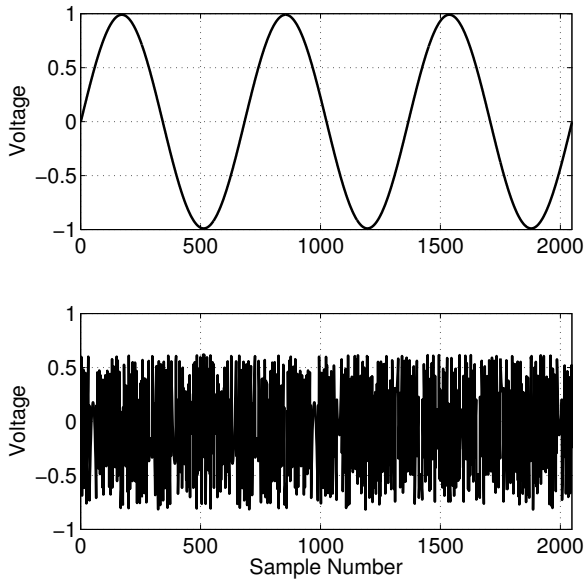

Fig. 4. Input to first MDAC and last-stage flash

Fig. 4 shows the input to the quantizer is no longer restricted between $-V_{ref}/2$ and $V_{ref}/2$. This therefore alters the performance of the pipeline, and overall performance depends on the kind of back-end flash used. The remainder of the section concentrates on the effects of offsets with different back-end flash architectures.

A. Traditional back-end flash architectures

In the presence of offsets, the performance of the pipeline ADC can still be ideal, as long as the quantization error does not leak beyond acceptable levels. For a 1.5b/stage MDAC with a 2-bit back-end flash, if we make sure that the quantization error does not leak beyond $\pm V_{ref}/2$, then the performance of the pipeline with offsets would match with that of an ideal pipeline ADC.

1) Effect of offset with back-end flash references $-V_{ref}/2, 0, +V_{ref}/2$: A regular 1.5 b/stage MDAC has a redundancy of $V_{ref}/4$ for its comparators, i.e. the offsets for the comparator in MDAC can vary between $-V_{ref}/4$ and $+V_{ref}/4$ and not effect the performance of the overall pipeline ADC. However, this is true only if the back-end ADC reference voltages are $-V_{ref}/2, 0, +V_{ref}/2$ exactly. In case the back-end flash references are not ideal, the overall performance of the pipeline degrades and the degradation in SNR would be directly correlated to the thresholds of the last stage flash.

2) Effect of offset with back-end flash references $-V_{ref}/4, +V_{ref}/4, +3V_{ref}/4$: In the case of using a back-end flash with references $-V_{ref}/4, +V_{ref}/4, +3V_{ref}/4$, the performance of the ADC is similar to that when using the references of $-V_{ref}/2, 0, +V_{ref}/2$. If the back-end flash references are ideal, then the SNR of the pipeline is ideal as long as the offset of the comparators in the MDACs lie in the permissible range ($-V_{ref}/4$ to $+V_{ref}/4$). In case the references of the back-end flash deviate from the ideal values, the performance of the overall pipeline degrades, but it is very similar to the case where the references are $-V_{ref}/2, 0, +V_{ref}/2$.

The above claim is verified using the following test setup. A pipeline ADC with 8x1.5 b/stage MDACs are used with a 2-bit flash as back-end. The offsets in the comparators of the MDACs are varied randomly (uniform distribution) from $-V_{ref}/5$ to $+V_{ref}/5$ over 500 different cases. Fig. 5 plots the histogram of the SNR when the back-end flash has no offsets in its threshold values.

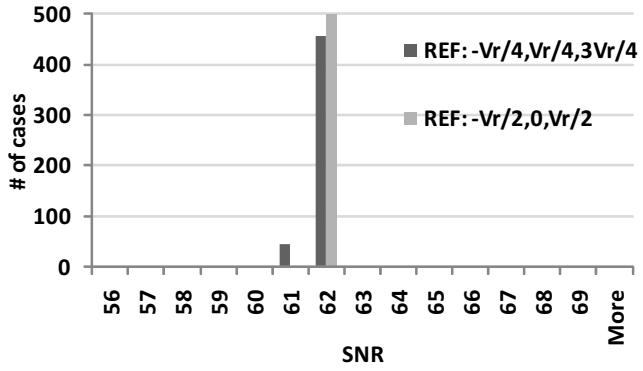

Fig. 5. Histogram of SNR for different offsets and ideal back-end

Fig. 5 shows the SNR for the two different back-end flash cases. It can be confirmed that if the back-end flash is ideal, then both the cases give similar performance with very little variation, even though the offset in comparators of the MDAC are as large as $\pm V_{ref}/5$.

In practical cases though, the back-end flash also has offsets and this adversely affects the performance of the pipeline. Fig. 6 compares the performance with the two different back-end flash stages, when offsets varying from $-V_{ref}/5$ to $+V_{ref}/5$ are present in the comparators of the 8x1.5b/stage MDACs and back-end flash (over 500 random cases).

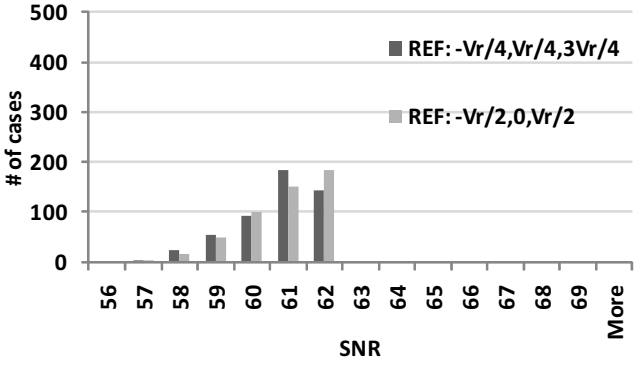

Fig. 6. Histogram of SNR for different offsets

The above plots (Fig. 5 and Fig. 6) confirm that the performance of the pipeline ADC is not effected by the exact

choice of the back-end flash. It should also be noted that if the back-end flash has no offsets, then the overall performance of the ADC is as good as the ideal one, even when the offsets present in the sub-ADCs of the MDAC are as large as $\pm V_{ref}/4$. Therefore, calibrating the offsets of the back-end flash alone could be highly beneficial.

B. Modified back-end flash architectures

In the case of using only one flash with a threshold of zero, the performance of the overall ADC cannot be matched with that of an ideal ADC (in the presence of offsets in front-end MDACs). This is because of quantization error leakage i.e. the quantization error leaks beyond $V_{ref}/2$. This would hence lead to degradation in performance. This is also true for the case when you use three comparators in the back-end but with thresholds of $-V_{ref}/4, 0, +V_{ref}/4$. In this case, once again the quantization error should be contained between $\pm V_{ref}/4$ (since it acts like a 3-bit back-end). However, this is not the case because of offsets in the MDAC and back-end flash.

Fig. 7 shows the histogram of the overall pipeline ADC with the two different modified back-end flash. Offsets varying from $-V_{ref}/5$ to $+V_{ref}/5$ are present in the MDAC and the back-end flash.

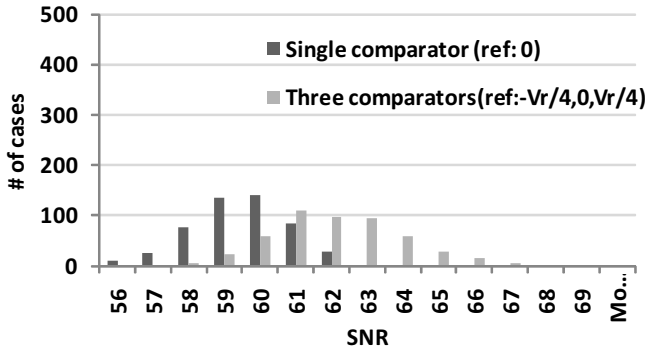

Fig. 7. Histogram of SNR for different offsets

The plot shows that using a single comparator, the SNR varies from 56 dB to 62 dB, whereas using 3 comparators (modified references), the SNR varies from 58 dB to 67 dB. However, if the last MDAC and the back-end flash are calibrated, then the performance can be improved tremendously. This is shown in Fig. 8, where offsets are present only in the first seven MDACs.

The results in Fig. 8 show that by calibrating the last MDAC and the back-end flash, the performance of the overall ADC can be closely matched with that of the ideal ones.

IV. Conclusion

This paper analyzes the back-end flash of a pipeline ADC and the need for accurate references in it. It shows that even with large offsets in the comparators of a MDAC, the performance of the pipeline ADC can be matched with an ideal ADC by calibrating a few comparators. Also, realizing the

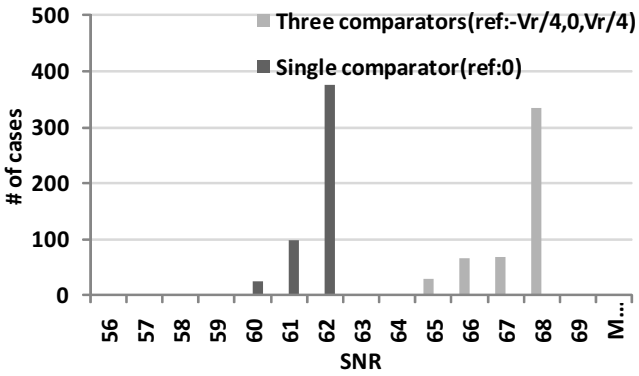

Fig. 8. Histogram of SNR for offsets present only in first seven MDACs

properties of the input to the back-end flash, modified back-end references are proposed and their results are compared with that of the traditional architectures. Table II summarizes the performance of a pipeline ADC with 8x1.5b/stage MDACs with different 2-bit back-end flash architectures. The two cases presented in the table are (1) Ideal case where no offsets are present in the comparators and (2) Uniformly distributed offsets lying between $\pm V_{ref}/5$ are present in all the comparators.

TABLE II
Performance for different back-end flash

Flash Architecture	Ideal Flash	Offsets (uniform $\pm V_{ref}/5$)
Conventional $(-V_{ref}/2, 0, V_{ref}/2)$	62 dB	59 dB (average)
Conventional $(\pm V_{ref}/4, 3V_{ref}/4)$	62 dB	59 dB (average)
Modified(0)	62 dB	58 dB (average)
Modified$(-V_{ref}/4, 0, V_{ref}/4)$	68 dB	62 dB (average)

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