Detection and Correction Methods for Single Event Effects in Analog to Digital Converters

Hariprasath Venkatram, Jon Guerber, Manideep Gande, and Un-Ku Moon

***Abstract*—This paper presents detection and correction methods for single event effects in analog to digital converters. Multi-path ADC based detection method is proposed for single event effects and bit error rate. Two correction schemes are proposed for single event effects based on multi-path ADC structure. 1) Two-path ADC based detection scheme with skip and fill algorithm based correction scheme. 2) Three-path ADC based detection scheme with majority voting based correction scheme. Advantages and limitations of both the methods are presented with simulation results. In particular, the three-path ADC can detect and correct for single event effects independent of repetition rate, magnitude of single event effects and the choice of data converter architecture. In three path ADC technique, the accuracy degradation is less than 1.7 dB or 0.28 bit for the Nyquist bandwidth for single event effects. Bit-Error Rate (BER) is effectively squared for three-path ADC as compared to a conventional ADC.**

***Index Terms*—Analog-digital conversion, bit error rate, metastability, pipeline ADC and multi-path ADC, radiation effects, radiation hardening by design, single event effects, single event upset, skip and fill interpolation, split-ADC technique, transient radiation effects.**

I. INTRODUCTION

DATA converters are ubiquitous blocks used to measure signals with a wide-range of bandwidths and resolutions. In particular, data-converters required for space electronics cover frequency ranges from few Hz to several hundreds of MHz and resolution ranges from 6 to 24 bits. No single data-converter architecture can satisfy this requirement in resolution and bandwidth at this juncture. Radiation hardening and BER reduction for such a block provides additional challenges to their design. In particular, single event effect (SEE) such as single event transients and single event upsets significantly degrade performance of the data converters [1]. Conventional radiation hardening methods for data-converters are architecture specific and often involve extensive simulation of circuit blocks with modified SPICE models [1], [18] and device level simulations. Therefore, it is fair to say that architecture independent radiation hardening and BER reduction techniques for data converters are desirable. Also, high level modeling and simulation methods will enable fast verification of extensive device and circuit simulations. Such techniques will enable reusable and robust design practices for building and testing data-converters. Ideally, these techniques should achieve this without any additional area or power penalty to the data-converter design.

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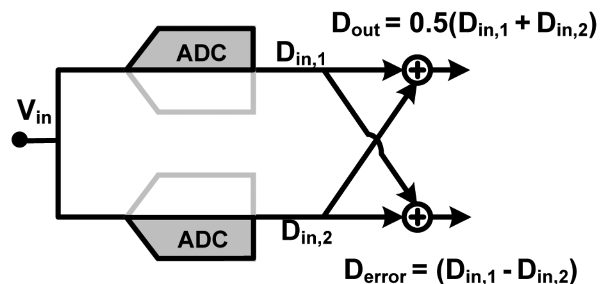

Fig. 1. Split-ADC technique.

In digital system design, triple modular redundancy (TMR) is extensively used for control and data paths to provide radiation hardening against single event upsets (SEU) [1]. However, this method suffers from area, power and performance penalties. A mixed signal design equivalent to the digital TMR technique is the multi-path ADC technique. This multi-path ADC technique enables a high level modeling, robust detection and correction method for SEE errors in an analog to digital converter. This multi-path ADC technique retains the benefit of digital TMR for radiation hardening and BER reduction without the penalties of analog area, power and performance.

Section II introduces split ADC technique, two-path and three-path ADC schemes. Section III analyzes system level modeling of SEE in analog to digital converter. Single event effects are discussed for a pipelined ADC and the need for correction methods is emphasized. Section IV describes the two-path ADC detection scheme with the skip and fill correction scheme. Section V elaborates on the three-path ADC detection scheme with the majority vote based correction method. Section VI briefly discusses the improvement in bit-error rate obtained from multi-path ADC technique and Section VII concludes the paper.

II. MULTI-PATH ADC TECHNIQUE

The multi-path ADC technique is an extension of the split-ADC technique [6]–[10] which is widely used for calibration of analog imperfections in data-converters. Here, we extend this technique to detect and correct single event effects and improve bit-error-rate in data-converters. This technique simplifies modeling, detection and correction in analog to digital converter.

A. Split-ADC Technique

Every capacitor and transconductance or opamp is split into two smaller pieces as shown in Fig. 1. The thermal noise power contribution increases by a factor of two due to this scaling.

Fig. 2 shows the noise model for the split-ADC. $V_{t,1}$ and $V_{t,2}$ represents the thermal noise contribution from the analog section of the split-ADC. $V_{q,1}$ and $V_{q,2}$ represents the quantization

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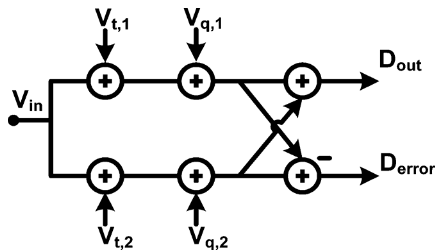

Fig. 2. Equivalent noise model.

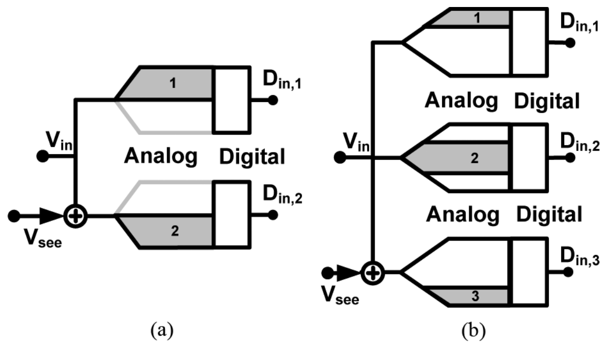

Fig. 3. a) Two-path and b) three-path ADC.

noise of the split-ADC. It can be readily observed that the averaged output, D_{out}, has the same signal to noise ratio of the combined ADC.

D_{out} contains the averaged output of the split-ADC and D_{error} contains information about the mismatch between the two channels. The signal content is removed in D_{error} and any anomaly between the channels can be detected from this digital error signal. In this application, along with the mismatch between the two-paths, single event effects and bit-error rates can be detected and corrected. Further details regarding the split-ADC technique can be found in [6]–[8]. As shown in Fig. 3, the digital section is the overhead for the split-ADC technique. The analog section made up of transconductors and capacitors does not increase in area or power.

B. Multi-Path ADC

Fig. 3(a) shows the two-path and Fig. 3(b) shows three-path ADC implementation. The analog portion of the ADC such as opamps, capacitors and comparators sized for thermal noise are split into equal parts. The two-path ADC is implemented in the same manner as a split-ADC while the three-path ADC is implemented by dividing the analog portion of the ADC into three smaller pieces and replicating the digital section. The shaded region represents the reduced size of each path obtained by splitting the analog blocks of the ADC built for thermal or quantization noise. The combined output of the multi-path ADC is obtained by taking the average of each ADC output $(D_{in,1}, D_{in,2}, \ldots)$.

The multi-path ADC technique not only allows calibration for gain and offset error but also provides digital detection and correction of single event effects and an improved bit-error rate in ADCs. The detection and correction of single event is achieved by monitoring the digital outputs $(D_{in,1}, D_{in,2}, \ldots)$ of the multi-path ADC. The multi-path ADC digital output carries information about a single event effect or bit-error rate from all possible internal nodes of the ADC from each path. Therefore, a simple comparison of digital output among the different paths against a digital threshold allows us to detect and correct SEE/BER.

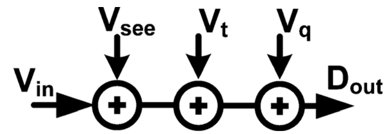

Fig. 4. Equivalent noise model for SEE.

Multi-path ADC technique can be thought of as a mixed signal version of the digital TMR. Thanks to the multi-path ADC technique, the analog section of the ADC does not see any area increase as compared to their digital TMR counterpart. The advantages of the multi-path ADC technique are summarized as follows: 1) Digital detection mechanism for SEE and bit error rate. 2) Real time correction methods based on digital outputs. 3) The detection and correction methods are independent of data converter architecture making it a robust and re-usable solution.

III. Single Event Effect in Analog to Digital Converter

Literature survey of SEE in analog to digital converter reveals a Gaussian model for SEE from the observed data [11]–[15]. Thanks to the multi-path ADC technique, digital detection of SEE/BER enables fast and accurate high level modeling using this Gaussian model. By studying the digital output, we can monitor the single event error from internal nodes of the data converter that affect the digital output. A conventional technique for studying the single event effects would involve device level simulation or simulation with modified SPICE models [13], [15]. In this conventional approach, critical nodes have to be identified and studied extensively through circuit and device simulators. Such methods are time consuming for a bigger system like a data converter and are computationally intensive to study the effects from all the blocks of a data converter. Unlike the conventional method, the multi-path ADC technique is independent of the data converter architecture and is amenable towards existing macro-modeling techniques for analog to digital converter. The digital detection is more efficient than analyzing the single event effects by studying transient voltage or current waveforms at a critical node in a given data converter. In the following sections, system level model for SEE, an application of SEE macro-model in a pipelined ADC, simulation results of SEE in a pipelined ADC and the need for detection and correction methods are explained in detail.

A. System Level Model for SEE

Fig. 4 shows a noise model for the ADC including an SEE noise source. V_{SEE} is a Gaussian random noise source for modeling SEE. V_t and V_q are Gaussian and uniform random noise sources for modeling thermal and quantization noise respectively.

The derivation of the random voltage source for single event effect is described in Appendix A. Signal to noise ratio for a given standard deviation (σ_{see}), repetition rate (N_{rep}) and observation window (N_{window}) is shown in (1). The combined signal to noise ratio along with the thermal and quantization noise is shown in (2), where $E(V_t^2)$ and $E(V_q^2)$ represent thermal and quantization noise power contribution respectively. The derivation for (1) and (2) is provided in Appendix A.

$$SNR_{SEE} = \frac{V_{rms}^2 . N_{window}}{\sigma_{see}^2 . N_{rep}} \tag{1}$$

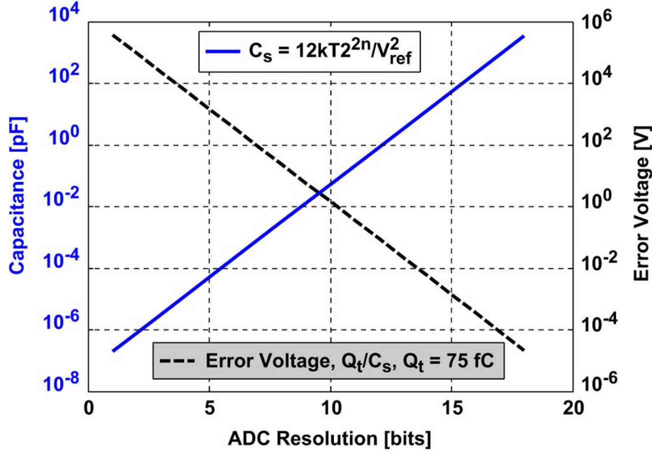

Fig. 5. Capacitance and error voltage vs. ADC Resolution.

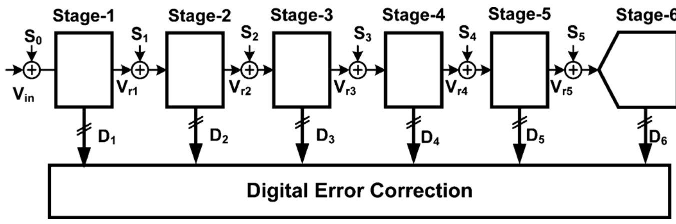

Fig. 6. Pipelined ADC model.

$$\mathrm{SNR_{total}} = \frac{\mathrm{V_{rms}^2}}{\frac{\sigma_{\mathrm{see}}^2.\mathrm{N_{rep}}}{\mathrm{N_{window}}} + \mathrm{E}(\mathrm{V_t^2}) + \mathrm{E}(\mathrm{V_q^2})}. \quad (2)$$

As shown in Fig. 4, SEE can be modeled as an error voltage source. The error voltage $(\mathrm{V_{see}})$ for a given ADC resolution (n), charge transferred $(\mathrm{Q_{see}})$ and reference voltage $(\mathrm{V_{ref}} = 1.2\ \mathrm{V})$ is given by (3) and (4).

$$\mathrm{C_s} = \frac{12\mathrm{kT}.2^{2\mathrm{n}}}{\mathrm{V_{ref}^2}} \quad (3)$$

$$\mathrm{V_{see}} = \frac{\mathrm{Q_{see}}}{\mathrm{C_s}} = \frac{\mathrm{Q_{see}}.\mathrm{V_{ref}^2}}{12\mathrm{kT}.2^{2\mathrm{n}}}. \quad (4)$$

Where $\mathrm{C_s}$ is the minimum sampling capacitance in Farad, k is the Boltzmann's constant and T is the temperature in Kelvin. The error voltage plot in Fig. 5 shows that the single event effect can saturate an ADC up to 10 bits and significantly reduce the dynamic range above 10-bit resolution. It can be observed from Fig. 5, that the commonly used radiation hardening technique of increasing the capacitor value $(\mathrm{C_s})$ to decrease the transient effect will not only increase area and power consumption of the system but also reduce the maximum achievable sample rate of the system [2], [3], [14].

B. SEE Model for a Pipelined ADC

The single event effect is modeled as a Gaussian random voltage source $(\mathrm{S_0} - \mathrm{S_5})$, [14]. The above modeling method is applied to a 12-bit pipelined ADC macro-model to study the single event effects from switches and amplifiers. The 12-bit pipelined ADC consists of five 2.5-bit stages followed by a 3-bit flash ADC as shown in Fig. 6. Each stage is made up of a sub-ADC, DAC and an amplifier as shown in Fig. 7.

Based on 12-bit noise and matching requirements, the typical input sampling capacitor is 2 pF and feedback capacitor of 500 fF, [16], [17]. A capacitor scaling factor of 2 is applied for matching considerations for the four stages resulting in feedback capacitors of 250 fF, 125 fF, and 62.5 fF for stages 2, 3, and 4 respectively. The fifth stage is a replica of stage-4 with feedback capacitor of 62.5 fF.

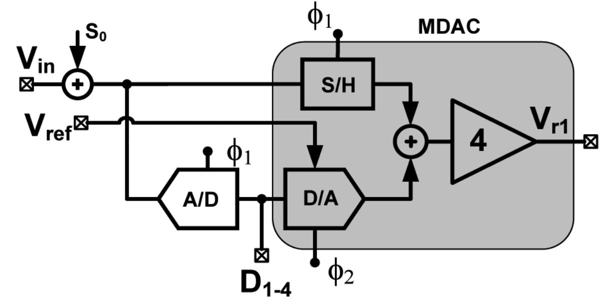

Fig. 7. Stage-1 block diagram.

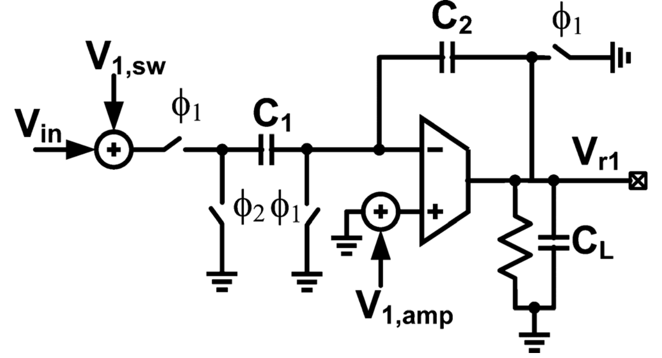

Fig. 8. Switched capacitor amplifier.

Fig. 8 shows a generic switched capacitor amplifier used in a pipeline ADC with non-overlapping clock phases (Φ_1 and Φ_2). The SEE for the switches can modeled by an equivalent random voltage source $(\mathrm{V}_{1,sw})$ and the SEE for the amplifier is modeled by an input referred random voltage source $(\mathrm{V}_{1,amp})$. The derivation for the input referred random noise source [18], using the double exponential current source model, is similar to conventional noise analysis. Appendix B discuss the derivation and limitations of the macro model used. Appendix C discusses about SEE noise model for an amplifier. Charge conservation at the inverting input terminal of the amplifier is used to derive the output voltage $(\mathrm{V_{out}})$. Equation (5) shows the output voltage of the amplifier with single event error source. Equation (5) is then re-written in terms of charge transferred in (6). From (6), we can observe that the single event effect on the output voltage depends on the feedback capacitance and the net charge transferred by the particle's energy. Fig. 9 shows the RMS output voltage of an amplifier for a single event effect in one of the sampling switches.

$$\mathrm{V_{out}}[\mathrm{n}] = \frac{\mathrm{C_1}}{\mathrm{C_2}}\mathrm{V_{in}}[\mathrm{n}] + \mathrm{V}_{1,amp}.\left(1+\frac{\mathrm{C_1}}{\mathrm{C_2}}\right) + \mathrm{V}_{1,sw}.\frac{\mathrm{C_1}}{\mathrm{C_2}} \quad (5)$$

$$\mathrm{V_{out}}[\mathrm{n}] = \frac{\mathrm{C_1}}{\mathrm{C_2}}\mathrm{V_{in}}[\mathrm{n}] + \frac{\mathrm{Q_{see,amp}}}{\mathrm{C_{in,amp}}}\left(1+\frac{\mathrm{C_1}}{\mathrm{C_2}}\right) + \frac{\mathrm{Q_{see,sw}}}{\mathrm{C_2}}. \quad (6)$$

The above model for the amplifier is used in the MDAC for every stage in the pipeline ADC shown in Fig. 7. The voltage magnitude of the single event error source for each stage depends on the random charge transferred and the capacitance of the corresponding pipeline stage (1–6). Equation (7) shows the

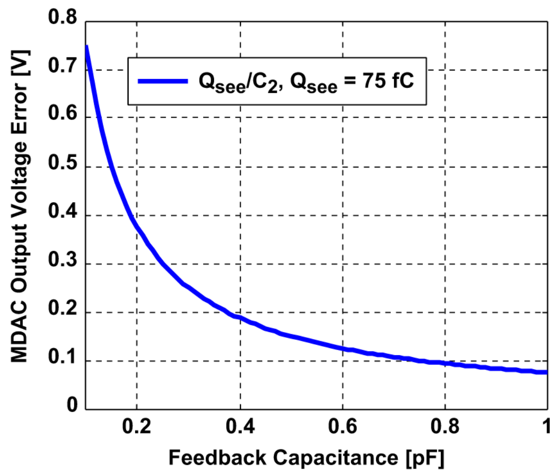

Fig. 9. MDAC output voltage change due to SEE.

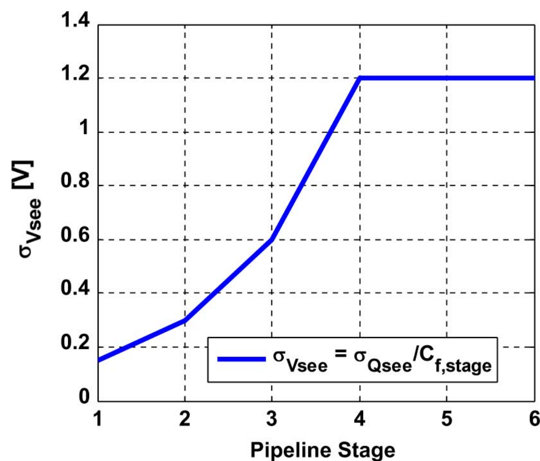

Fig. 10. Standard deviation of single event source.

error voltage source derived from a single event particle's energy source for the different stages of the pipeline ADC ($S_0 - S_5$).

$$\sigma_{\rm see,input} = \frac{\sigma_{\rm q,see}}{C_{\rm f,stage} . G_{\rm eff,input}}. \tag{7}$$

where $C_{\rm f,stage}$ is the feedback capacitance for each stage (C_{f1-5}) and $G_{\rm eff,input}$ is the input referred gain. It is instructive to note that the capacitor scaling factor of 2 along with the inter-stage gain of 4 reduces the SEE error voltage introduced in the later stages. Fig. 10 shows the magnitude of the SEE error voltage source, ($S_0 - S_5$), derived from a Gaussian SEE error voltage source given by (7). Equation (1) can be re-written using (8) to obtain the signal to noise ratio due to the SEE error voltage source. With this error voltage source, (9) can be used to study the degradation in signal to noise ratio due to the SEE error voltage source.

$$E(V^2_{\rm see}) = \sigma^2_{\rm see,input} . \frac{N_{\rm rep}}{N_{\rm window}} \tag{8}$$

$$\mathrm{SNR} = \frac{V^2_{\rm rms}}{E(V^2_{\rm see})} = \frac{V^2_{\rm rms} . N_{\rm window}}{\sigma^2_{\rm see,input} . N_{\rm rep}}. \tag{9}$$

The position of the SEE error voltage source in the pipeline ADC, $S_0 - S_5$, and its repetition rate ($N_{\rm rep}$) was varied to study the effects on the signal to noise ratio. Each sample point in

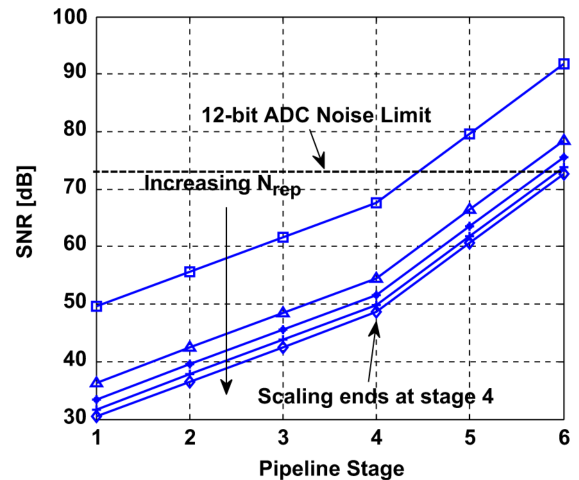

Fig. 11. SNR for repetition rates 1, 20, 40, 60, and 100 in ADC.

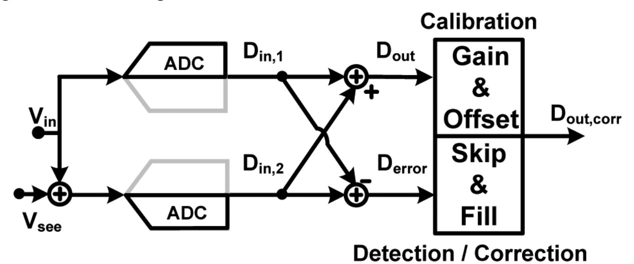

Fig. 12. Split-ADC with skip and fill correction.

Fig. 11 shows average signal to noise ratio of 100 runs. The simulation results were obtained by using the macro-model of Fig. 6 in MATLAB and the results obtained closely match the values derived using (9). The simulation results also confirms that the SEE in the later stages of the pipeline ADC has less impact on the SNR as compared to the SEE in the earlier stages. This can be readily observed from (7), Figs. 10 and 11. The input referred SEE error voltage, $\sigma_{\rm see,input}$, is reduced by the inter-stage gain, $G_{\rm eff,input}$, of the pipeline ADC. The SEE repetition rate was also varied to study the effect on SNR with a fixed observation window. Fig. 11 shows that even for small repetition rates of the SEE error SNR can significantly lower from the ideal value. This significant reduction in SNR, due to SEE in the signal path, is the motivation for the detection and correction schemes presented in the following sections.

IV. Two-Path ADC With Skip and Fill Algorithm

By introducing two identical paths using the split-ADC technique, the SEE can be detected by monitoring the digital output, $D_{\rm error}$, against a digital threshold. Fig. 12 shows the implementation of a two-path ADC with skip and fill algorithm [6]–[10]. $D_{\rm error}$ is used to detect the SEE error and the skip and fill algorithm is used for replacing the corrupt sample. The skip and fill algorithm is a non-linear interpolation algorithm which is superior to the linear interpolation methods in terms of the number of taps required for a given accuracy requirement.

A. Detection and Correction Using Skip and Fill Algorithm

The skip and fill algorithm uses a non-linear interpolation method to fill the missing or corrupted sample. The details of the algorithm can be found in [9], [10]. The SEE detection scheme consists of a simple bit by bit logical comparison of $D_{\rm error}$, against a digital threshold. The skip and fill block receives two

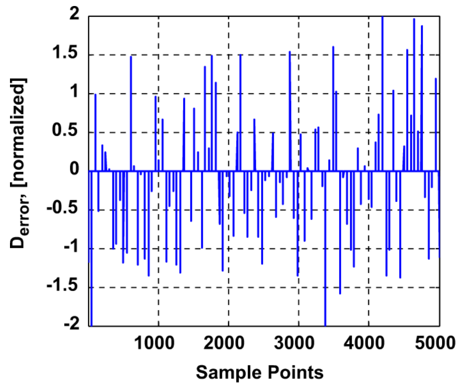

Fig. 13. D_{error} vs. sample points, $N_{rep} = 100, N_{window} = 4096$.

digital outputs, D_{error} and D_{out}, from the split-ADC and generates the corrected output, $D_{out,corr}$. If the magnitude of D_{error} is larger than the set digital threshold, the output (D_{out}) is replaced with the interpolated value using (10b). Otherwise, (D_{out}) is passed on to the output with latency as given by (10a). The interpolation and the SEE error correction is performed only if the SEE error is detected, leading to power efficient use of correction hardware.

$$D_{out,corr}(m) = D_{out}(m) \quad \text{if } D_{error} < 2\text{LSB} \quad (10a)$$
$$= D_{inter}(m) \quad \text{if } D_{error} > 2\text{LSB}. \quad (10b)$$

B. Simulation Results

A 12-bit pipelined ADC macro-model shown in Fig. 6 was used in the two-path ADC technique. For the skip and fill correction method, a 40-tap interpolation filter was used with a 4096 sample length observation window. The standard deviation of the SEE error source was 0.4 V. The two-path ADC was calibrated for gain and offset error before simulating SEE errors.

The output, D_{error}, used for the SEE error detection, the uncorrected (D_{out}) and corrected output ($D_{out,corr}$) are shown in Figs. 13, 14, and 15 respectively. Equation (10) was used to identify and correct SEE errors using the skip and fill interpolation. In order to study the limitations of the interpolation based skip and fill correction scheme, the repetition rate of the SEE error source and the input signal frequency were varied. The resulting signal to noise ratio of the corrected output for the different SEE error repetition rates and the input signal frequency is shown in Fig. 16. The accuracy of the interpolated sample decreases with the increase in the input signal frequency. Even for a small SEE error repetition rate, the skip and fill interpolation based SEE error correction bandwidth is limited to 30% of the Nyquist frequency range. Another theoretical limitation occurs when the repetition rate of SEE error is more than 10% percent of the window of observation. In this case, SNR degradation occurs due to uncorrected SEE errors being used for interpolation. These drawbacks can be eliminated by implementing the three-path ADC correction method.

V. Three-Path Split-ADC Correction Algorithm

SEE is a localized event and the probability of the SEE error equally affecting more than one path in a three-path ADC in the same sample is negligible. The three path ADC technique splits the ADC into three equal smaller parts to perform SEE error detection and correction as shown in Figs. 17 and 18. The gain and offset error correction is performed as given by [6] and [7]. The SEE error correction is discussed below.

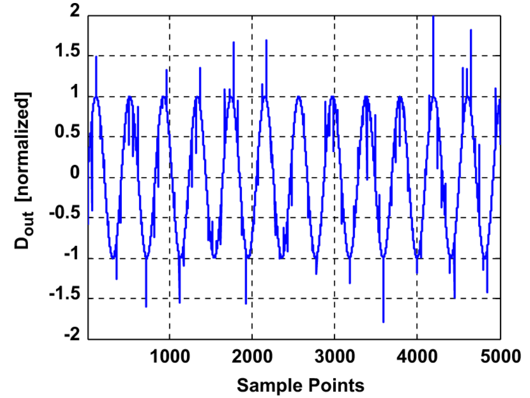

Fig. 14. D_{out} vs. sample points, $N_{rep} = 100, N_{window} = 4096$.

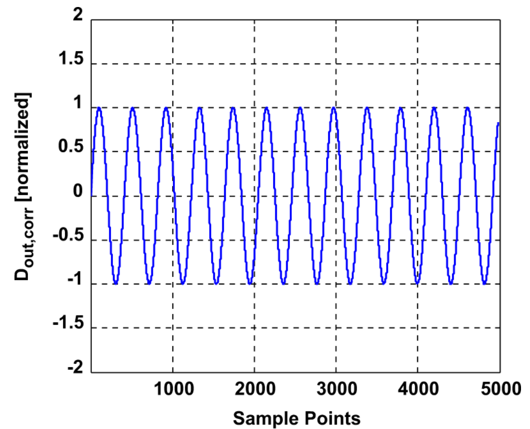

Fig. 15. $D_{out,corr}$ vs. sample points, $N_{rep} = 100, N_{window} = 4096$.

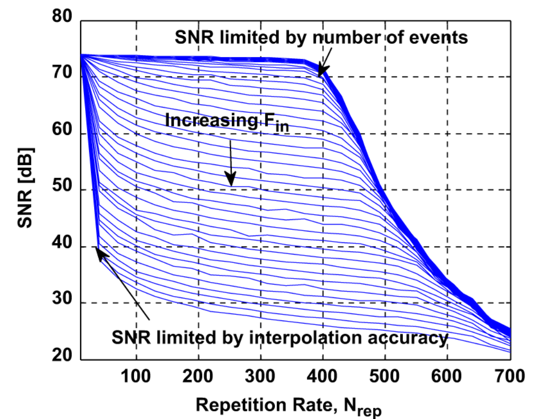

Fig. 16. Limitations of two-path ADC correction method.

A. Correction by Majority Voting

Fig. 18 shows implementation of the three-path SEE error detection and correction scheme. SEE error is a localized event and it affects only one of the three paths in the three-path ADC. Therefore, the SEE error detection involves a simple comparison of each of the error terms against a digital threshold which can be programmed for different environments. The minority term among the three error terms provides the two un-corrupted channels. SEE Correction involves dropping the corrupt channel output and averaging the output from the remaining two un-corrupted channels. This correction method can be implemented

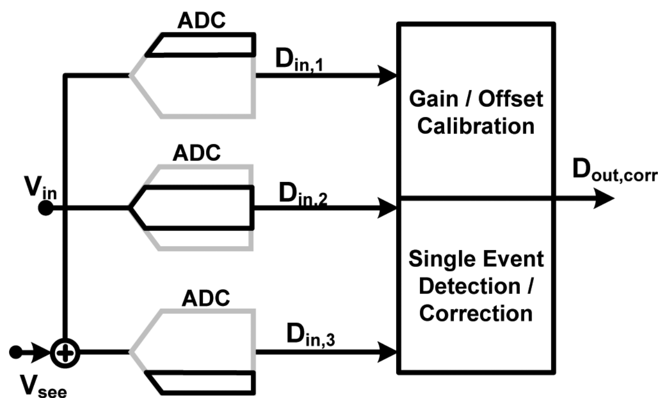

Fig. 17. Three-path split-ADC.

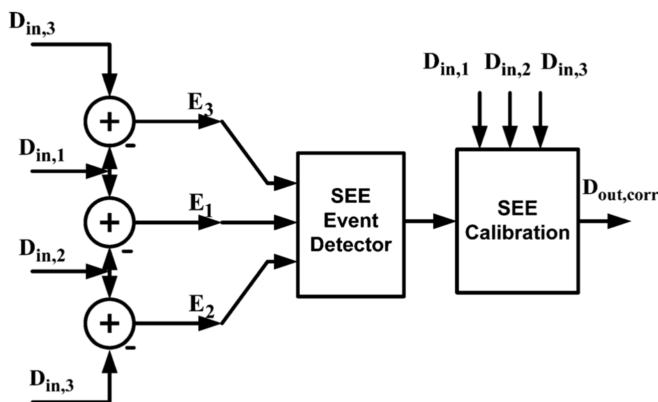

Fig. 18. SEE detection and correction.

using simple digital logic and is explained below.

$$\begin{aligned} \mathrm{D_{out,corr}} &= \frac{1}{2}\left(\mathrm{D_{in,3}}+\mathrm{D_{in,1}}\right); \mathrm{E_1, E_2} > \mathrm{3LSB, E_3} < \mathrm{3LSB} \\ \mathrm{D_{out,corr}} &= \frac{1}{2}\left(\mathrm{D_{in,1}}+\mathrm{D_{in,2}}\right); \mathrm{E_2, E_3} > \mathrm{3LSB, E_1} < \mathrm{3LSB} \\ \mathrm{D_{out,corr}} &= \frac{1}{2}\left(\mathrm{D_{in,2}}+\mathrm{D_{in,3}}\right); \mathrm{E_3, E_1} > \mathrm{3LSB, E_2} < \mathrm{3LSB} \\ \mathrm{D_{out,corr}} &= \frac{1}{3}\left(\mathrm{D_{in,1}}+\mathrm{D_{in,2}}+\mathrm{D_{in,3}}\right); \mathrm{E_1, E_2, E_3} < \mathrm{3LSB}. \end{aligned} \quad (11)$$

B. Simulation Results

For this example, the standard deviation of the SEE error source was 0.4 V and the observation window length was 4096. The SEE error detection threshold for single event effect was arbitrarily set to 2 LSBs. Fig. 19 shows the outputs of individual channels. During the first 1500 samples, first channel, $\mathrm{D_1}$, is corrupted. $\mathrm{D_2}$ is corrupted for the next 1500 samples and $\mathrm{D_3}$ is corrupted for the remaining samples in the simulation. Fig. 20 shows the error terms generated using (11). The error terms in Fig. 20 contains information about the corrupt channel. In particular, the minority term of $\mathrm{E_2}$ for the first 1500 samples identifies that the two uncorrupted channels are $\mathrm{D_2}$ and $\mathrm{D_3}$. This can be observed from Fig. 20. The corrected output, $\mathrm{D_{out,corr}}$, will be the average of $\mathrm{D_2}$ and $\mathrm{D_3}$ as given by (11). The corrected output is obtained from (11) by dropping the corrupted channel is $\mathrm{D_1}$, shown in Fig. 21. Similarly, minority terms of $\mathrm{E_3}$ and $\mathrm{E_1}$ show that the corrupted channels are $\mathrm{D_2}$ and $\mathrm{D_3}$ respectively.

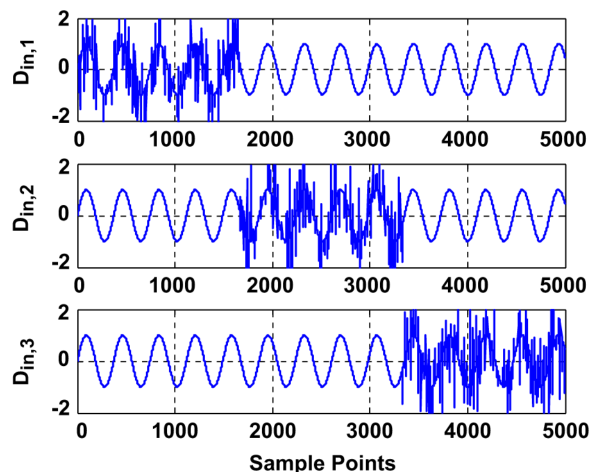

Fig. 19. Normalized individual channel outputs.

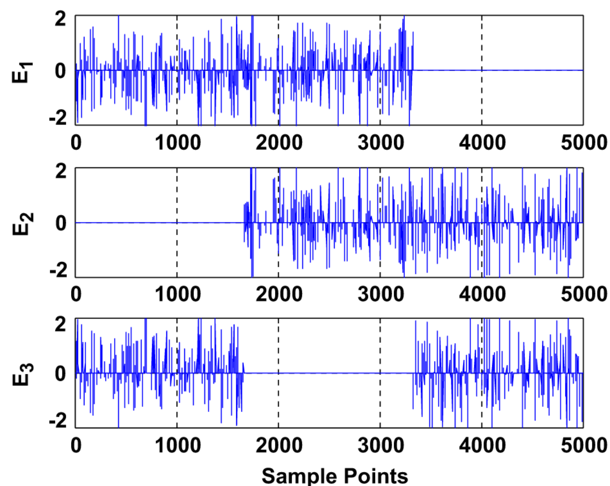

Fig. 20. Normalized error terms.

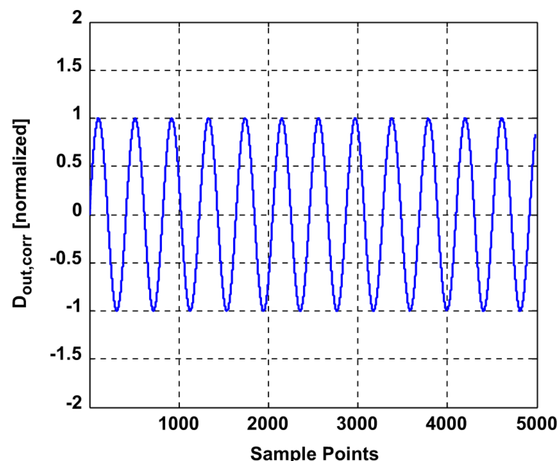

Fig. 21. Three-path ADC corrected output.

C. Advantages of Majority Voting Based Correction

The advantages of this correction scheme are as follows: effective correction for the entire Nyquist bandwidth, simple digital correction, programmable SEE detection threshold, and real-time correction without any latency. Fig. 22 shows the corrected output accuracy for different repetition rates. For each repetition rate, N, SNR was obtained by averaging 100 simulation runs.

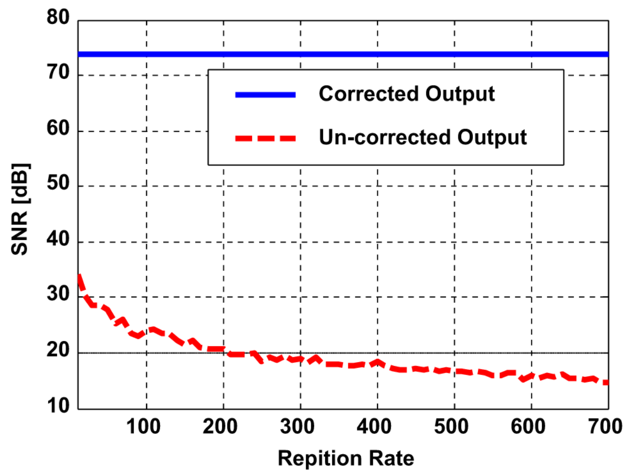

Fig. 22. SNR vs. frequency and $N_{rep} = 10$ to 700.

The artificially high repetition rate was used to point out differences between two-path and three-path ADC correction schemes. Needless to say, input frequency or the repetition rate has no effect on the thee-path ADC correction scheme. The efficacy of this correction scheme can be seen from Fig. 22. By dropping one of the corrupt channels, the signal to noise ratio drops by 0.28 bit from its ideal value. This is due to the fact that the noise power from the two channels is $6 \times P_{Nsingle}$, whereas the signal power is $4 \times P_{sig}$, where $P_{Nsingle}$ and P_{sig} is the noise and signal power of the single channel ADC respectively. This causes the signal to noise ratio of the corrected output to drop by a factor of $10 \times \log(4/6)$ or 1.7 dB or 0.28 bit from its ideal value. The performance degradation is independent of number of single event errors as compared to two-path ADC correction scheme. The limitation to this correction scheme is that the single event effect cannot happen in more than one channel simultaneously.

D. Comparison of Single, Two-Path and Three-Path ADC

Table I compares the different aspects of the single, two-path and three-path ADC. Thanks to the multi-path ADC technique, the signal to noise ratio is the same for single, two and three path ADC. The core analog area consisting of capacitors and transconductors remain the same due to the multi-path ADC technique. The signal and power routing area will marginally increase as compared to the single-path ADC. This routing area increase is marginal as compared to triplicating the initial single path ADC. SEE correction blocks and any digital logic in the single path ADC is the overhead in the multi-path ADC implementation.

The fractional interpolation filter used for the two-path ADC and the majority (minority) voting correction block of the three-path ADC is the additional digital hardware required for SEE correction in the multi-path ADC. The two-path ADC along with the SEE correction block restores the performance of the ADC from less than 6 bit without SEE correction to 12 bit for half of the Nyquist bandwidth ($f_s/4$). The three-path ADC with majority voting correction scheme restores the performance for the entire Nyquist bandwidth ($f_s/2$). It is instructive to understand that the correction accuracy and bandwidth offered by three-path ADC cannot be matched by interpolation based correction schemes. The correction accuracy deteriorates rapidly for input frequency above $f_s/4$ and is not favorable for Nyquist rate ADCs.

TABLE I
COMPARISON OF SINGLE, TWO-PATH AND THREE-PATH ADC PERFORMANCE

Parameter	Single-Path	Two-Path	Three-Path
SNR w/o SEE	12 bit	12 bit	12 bit
Core Analog Area	Same	Same	Same
Digital Overhead	-	Interpolation and Digital Logic	Majority Voting and Digital Logic
SEE Correction Method	-	Skip and Fill	Majority Voting
Correction BW	None	$f_s/4$	$f_s/2$
SNR w/ SEE and SEE correction	< 6 bit	12 bit	11.72

VI. BIT-ERROR RATE IN ADC

The comparators in the ADC introduce meta-stable events which manifests as bit-error-rate (BER) [19]. The conventional method to reduce meta-stability induced BER in an ADC is to increase the regeneration time of the comparator or introduce gain-stages before the regenerating latch to increase the input signal range to the regenerative latch [19]. A few architectural changes allow increased regeneration time for the comparator [19], [23]. Redundancy improves meta-stability induced bit-error rate in various pipeline ADC architectures [20], [21] as compared to successive approximation ADC [19] or cyclic/algorithmic ADC. The two-path and three-path ADC technique provides the same improvement as triple modular redundancy without area penalty. The bit-error rate, proportional to $e^{-T_{reg}/\tau}$, is squared and is equal to $e^{-2T_{reg}/\tau}$. In a three-path ADC, the majority voting based correction detects the channel with the bit-error and discards the output from the corrupted channel.

VII. CONCLUSION

Single event effects significantly degrade the performance of the data-converters. Inspired by the digital techniques, two correction methods were discussed. Both the methods do not suffer from core analog area or power penalties as compared to their digital counterparts owing to the multi-path ADC technique. The detection schemes are digital in nature and can be programmed for different environments and data converter architectures by modifying the digital threshold in the detection and correction blocks. The correction scheme involves replacing the corrupted sample altogether, rather than analyzing voltage transients, which enables a high level modeling approach to quickly evaluate the performance using a very few design parameters for SEE and the ADC involved. The multi-path ADC effectively squares the individual ADC's bit error rate performance and it is same as the conventional TMR implementation without the increase of analog area or power.

APPENDIX A

Signal to noise ratio for an ADC with single event Gaussian random noise source is derived as follows. Fig. 4 shows the model for the ADC with a single event noise source and quantization noise source. The quantization noise depends on the resolution (Δ) of the ADC and is uniform. SEE is modeled as a

Gaussian noise distribution with standard deviation of σ. Equation (12) is used to derive the signal to noise ratio with SEE, where V_{rms} is the signal energy and $E(X^2)$ is the energy of the random signal X. Equation (12) can be applied to the quantization noise and Gaussian single event noise source as shown in (12). However, the single event happens only N_{rep} times in a given observation window, N_{window}. Therefore, the noise energy is scaled by N_{rep}/N_{window}. Equation (13) shows the signal to noise ratio for Gaussian and the familiar quantization noise.

$$\begin{aligned} \mathrm{SNR} &= \frac{V_{rms,signal}^2}{E(X^2)}, \\ E(X_{uniform}^2) &= \frac{\Delta^2}{12}, E(X_{gaussian}^2) = \sigma^2 \\ \mathrm{SNR}_{see} &= \frac{V_{rms}^2.N_{window}}{\sigma_{see}^2 N_{rep}}, \mathrm{SNR}_{quant} = \frac{V_{rms}^2.12}{\Delta^2} \end{aligned} \tag{12}$$

$$\mathrm{SNR}_{combined} = \frac{V_{rms}^2}{\frac{\sigma_{see}^2.N_{rep}}{N_{window}} + \frac{\Delta^2}{12}}. \tag{13}$$

Appendix B

SEE is modeled as a noise current source shown in (14) as shown in Fig. 24[18], where Q_{see} is the ion charge transferred by the energy particle, α, β, τ are the constants derived from the device model. The sampled voltage on the capacitor C_s is shown in (15), where i_{see} represents the model for SEE current source, Q_{see} is the random charge transferred from the energy particle, α, β, τ are the constants derived from the device model, C_s is the sampling capacitor and T_s is the sampling rate.

$$i_{see} = \frac{Q_{see}}{\tau}\left(\exp\left(\frac{-\alpha.t}{\tau}\right) - \exp\left(\frac{-\beta.t}{\tau}\right)\right) \tag{14}$$

$$V_{th}[nT_s+0.5T_s] = V_{in}[nT_s+0.5T_s] + \frac{1}{C_s}.\int_0^{0.5T_s} i_{see}.dt \tag{15}$$

$$V_{see} \approx \gamma.\frac{Q_{see}}{C_s}. \tag{16}$$

However, SEE current source model is derived from a packet of charge delivered by the energy particle [18]. The integral shown in (15) describes the amount of charge transferred to the sampling capacitor. In general, the time constant of the modeled is much smaller compared the sampling-rate used for the system and can be simplified to (16), where γ is proportionality constant relating the packet of charge delivered by the energy particle and the voltage change V_{see}. As shown in Fig. 24, this current source charges a capacitor (C_s) for a given sampling period (T_s). The voltage change produced by this current source is directly related to the ion charge transferred by the energy particle and this can be derived as shown in (17), (18), and (19) at the bottom of the page. α, β, τ are derived from a specific device under consideration. α, β, τ used for the following discussion are 3, 4 and 12.5 ps respectively. Fig. 24 shows the error percentage as a function of T_s/τ. It can be observed that for ratios of Ts/τ greater than 20, the error in the approximation of (19) is less than 0.25%. In our discussion, we had assumed that the current pulse is ON for the entire sampling period $(0.5T_s)$. However, the above discussion indicates that within twenty time constants (τ) of the current pulse, 99.75% of the charge is transferred to the capacitor. In other words, if the sampling period $(0.5T_s)$ is larger than 20 time constants, the modeling error is less than 0.25%.

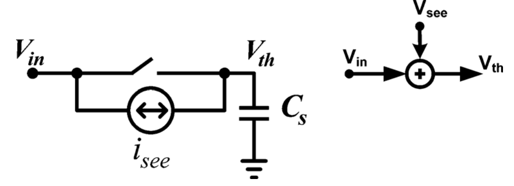

Fig. 23. Sample and hold.

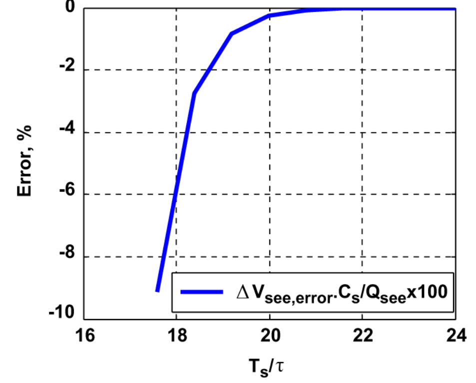

Fig. 24. Error percentage vs. T_s/τ.

Appendix C

The derivation for the input referred SEE noise follows the traditional noise analysis of a differential pair as shown

$$\begin{aligned} V_{see} &= \frac{1}{C_s}.\int_0^{0.5T_s} i_{see}.dt \\ &= \frac{Q_{see}}{C_s}\frac{\beta-\alpha}{\alpha\beta} + \frac{Q_{see}}{C_s\tau}\left(\frac{1}{\beta}\exp\left(\frac{-\beta.0.5T_s}{\tau}\right) - \frac{1}{\alpha}\exp\left(\frac{-\alpha.0.5T_s}{\tau}\right)\right) \end{aligned} \tag{17}$$

$$V_{see} = \gamma.\frac{Q_{see}}{C_s} + \Delta V_{see,error}, \gamma = \frac{\beta-\alpha}{\beta.\alpha} \tag{18}$$

$$\frac{\Delta V_{see,error}}{\frac{Q_{see}}{C_s}} = \frac{1}{\tau}\left(\frac{1}{\beta}\exp\left(\frac{-\beta.0.5T_s}{\tau}\right) - \frac{1}{\alpha}\exp\left(\frac{-\alpha.0.5T_s}{\tau}\right)\right) \tag{19}$$

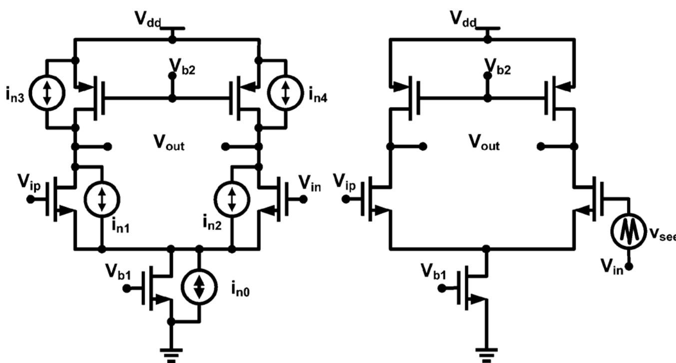

Fig. 25. Single stage amplifier with SEE noise sources.

in Fig. 25. The noise current sources $(\mathrm{i_{n0}} - i_{n4})$ model the single event effect. The tail current source noise $(\mathrm{i_{n0}})$ is a common-mode noise and it is rejected by the common-mode rejection ratio (CMRR) of the amplifier [16], [17]. The noise current sources $(\mathrm{i_{n1}} - \mathrm{i_{n4}})$ can be replaced by an equivalent input referred noise source $(\mathrm{v_{see}})$. The equivalent input referred noise is given by (20).

$$v_{see,in} = \frac{1}{g_{m,in}} \left(\sum_{p=1}^{4} i_{n,p} \right). \tag{20}$$

where $\mathrm{g_{m,in}}$ is the transconductance of the input pair in the quiescent state.

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